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In situ Silane Surface Passivation for Gate-First Undoped AlGaN/GaN HEMTs with Minimum Current Collapse and High-Permittivity Dielectric

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1. INTRODUCTION

Gallium nitride (GaN)-based materials are attractive for high power, high temperature, and high frequency applications [1], primarily due to their superior properties, such as large critical electric field, wide energy band gap E_G, and high electron mobility. However, one of the challenges faced by GaN High Electron Mobility Transistors (HEMTs) is current collapse, which is due to the presence of slow-acting trapping states between the gate and the drain of the device [2]. Various surface passivation techniques have been proposed using various dielectrics, such as Si_3N_4 [2], Al_2O_3 [3], etc, and different surface treatments, such as NH_3-plasma treatment [4]. In our previous study, we demonstrated the effectiveness of an *in situ* surface passivation technique comprising vacuum anneal (VA) and silane (SiH_4) treatment in a metal-organic chemical vapor deposition (MOCVD) chamber, using TaN/HfAlO/n-GaN MOS capacitors [5].

In this paper, the *in situ* VA and SiH_4 surface passivation technique was first demonstrated on undoped AlGaN/GaN MOS-HEMTs. Excellent DC characteristics with minimum current collapse at 300 K were obtained. In addition, DC characteristics at high temperatures were also studied in detail.

2. DEVICE FABRICATION

The process flow for fabricating the AlGaN/GaN MOS-HEMT structure is shown in Fig. 1. A 2-inch undoped $Al_{0.25}Ga_{0.75}N$(20 nm)/GaN(2 μm)/ on sapphire substrate was used. After active region formation using Cl_2-based reactive ion etching (RIE), pre-gate cleaning steps comprising HCl for native oxide removal followed by $(NH_4)_2S$ for *ex-situ* surface passivation to prevent native oxide growth [5] were performed.

After pre-gate cleaning, the wafers were quickly loaded into a MOCVD multi-chamber gate cluster system for *in situ* surface passivation: baking at 300 ºC under high vacuum for decomposition of any native oxide, and SiH_4 treatment at 400 ºC for surface passivation. Then, MOCVD high-*k* dielectric (HfAlO) (20 nm) was deposited. Post Deposition Anneal (PDA) at 500 ºC for 60 s in N_2 ambient was then performed to improve the quality of the as-deposited HfAlO film, followed by reactive sputter deposition of TaN metal and gate patterning. Al (71 nm)/Ti (30 nm) were deposited using an E-Beam evaporator and patterned using a lift-off process. An alloying process at 650 ºC for 30 s in N_2 ambient formed ohmic contacts on GaN. Finally, the fabrication process was completed with a forming gas anneal at 420 ºC for 30 mins.

3. RESULTS AND DISCUSSION

Fig. 2 shows the current-voltage (*I-V*) characteristics, at different spacings, on the fabricated transfer length method (TLM) test structure which was fabricated along with the device fabrication, after annealing at 650 °C for 30 s. Excellent *I-V* characteristics were obtained, with sheet resistance (R_{sh}) of 380 Ω/□, and specific contact resistivity (ρ_c) of 1.5×10^{-3} Ω cm^2.

Fig. 3 shows the capacitance-voltage (*C-V*) curve (300 K) measured at 1 MHz for the fabricated MOS-HEMT. A sharp transition from depletion to accumulation is observed, demonstrating the high quality of the interface between HfAlO and AlGaN. In accumulation, the total capacitance could be expressed as $1/C_{total} = 1/C_{HfAlO} + 1/C_{AlGaN} + 1/C_{IL}$. From the measured value of C_{total} of 66.4 pF, and the calculated C_{HfAlO} and C_{AlGaN} of 200.1 pF (thickness 20 nm, $\varepsilon_{HfAlO} = 18$) and 106.1 pF (thickness 20 nm, $\varepsilon_{AlGaN} = 9.5$), respectively, the interfacial layer (IL) thickness is deduced to be around 0.6 nm if SiO_2 is assumed for the IL ($\varepsilon_{SiO2} = 3.9$). This estimate agrees well with the IL thickness measured using TEM in our previous study [5].

I-V characteristics (300 K) of a gate first undoped AlGaN/GaN MOS-HEMT with a 2 μm gate length (L_G) are shown in Fig. 4 and 5. This MOS-HEMT has a threshold voltage (V_{th}) of - 4.9 V using a linearly scale drain current (V_D = 1 V), and a subthreshold Swing (*SS*) of 97 mV/decade. A maximum transconductance (g_m) of 80 mS/mm was obtained (V_D = 5 V). Good saturation and pinch-off device characteristics can be observed (Fig. 6). The drain current collapse at a given $V_G - V_{th}$ is defined as the current reduction per unit increase in drain voltage, i.e. $\Delta I_D/\Delta V_D$. Fig. 7 compares the current collapse in this work with those of recently published results (depletion mode MOS-HEMTs with L_G between 0.8 and 2 μm).

Fig. 8 to 11 show the DC characteristics of undoped AlGaN/GaN MOS-HEMTs (L_G = 2 μm) measured at high temperatures. As temperature increases from 300 K to 460 K, saturation drain current (I_{Dsat}) decreases from 0.4 A/mm to 0.23 A/mm at $V_G - V_{th}$ = 6.5 V, off-state current increases from 1.5×10^{-8} A/mm to 1.2×10^{-7} A/mm at $V_G - V_{th}$ = -2.5 V, *SS* increases from 97 mV/decade to 289 mV/decade, V_{th} becomes more negative at a rate of 0.62 mV/°C, and mobility drops dramatically. I_{Dsat} reduction is mainly due to the decrease in mobility as the temperature increases.

4. SUMMARY

In summary, an *in situ* surface passivation technology comprising vacuum anneal and SiH_4 treatment was integrated in the fabrication of undoped AlGaN/GaN MOS-HEMTs. Excellent DC characteristics with minimum current collapse at room temperature were obtained. DC characteristics at high temperatures were also investigated.

Acknowledgement.

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- AlGaN/GaN wafer on 2” sapphire substrate
- Active region formation using RIE (Cl_2)
- Gate stack formation
  - *Pre-gate cleaning*:
    HCl, $(NH_4)_2S$
  - *In-situ passivation*:
    Vacuum annealing and SiH_4 treatment
    High-k dielectric deposition and PDA
    Gate deposition and patterning
- Contact patterning and Al/Ti deposition
  by E-beam
- Lift-off process and ohmic contact alloying
- Forming gas anneal

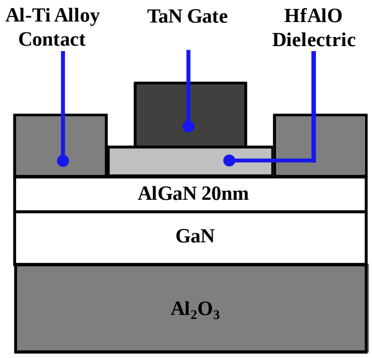

Fig. 1. (a) Left: Process flow for fabrication of the AlGaN/GaN MOS-HEMT. (b) Right: Schematic view of the AlGaN/GaN MOS-HEMT structure.

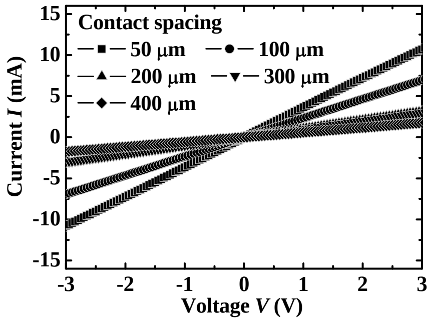

Fig. 2. Current-voltage (*I-V*) characteristics at different contact spacings on the TLM structure after annealing at 650°C for 30 s .

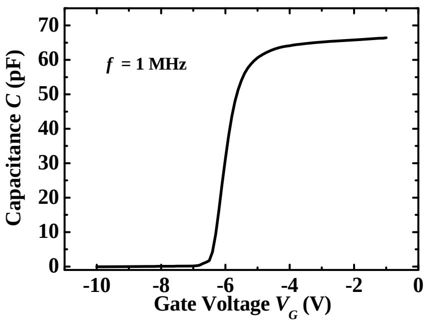

Fig. 3. Measured Capacitance-Voltage (*C-V*) characteristic of the AlGaN/GaN MOS-HEMT with VA and SiH_4 treatment.

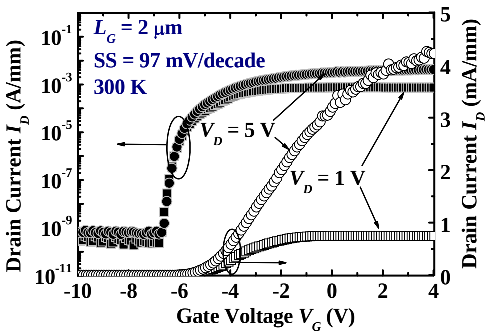

Fig. 4. I_D-V_G output characteristics of AlGaN/ GaN MOS-HEMT with VA and SiH_4 treatment. Low *SS* of 97 mV/decade was achieved at 300 K.

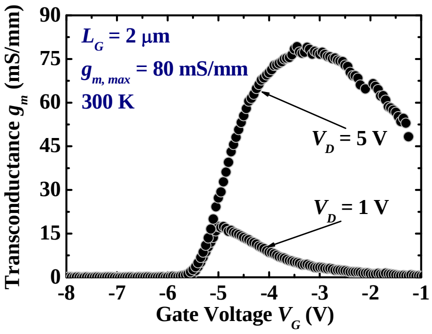

Fig. 5. g_m-V_G transfer characteristics of AlGaN/GaN MOS-HEMTs with VA and SiH_4 treatment.

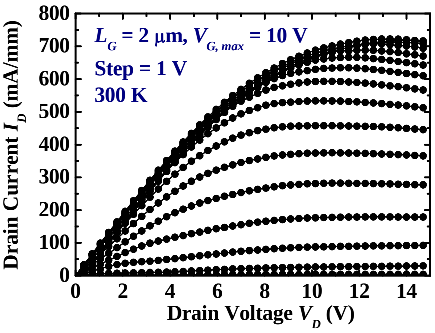

Fig. 6. I_D-V_D characteristics of AlGaN/GaN MOS-HEMT with VA and SiH_4 treatment.

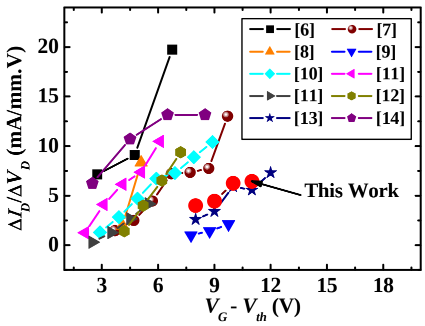

Fig. 7. Current collapse comparison of our work with recent published results.

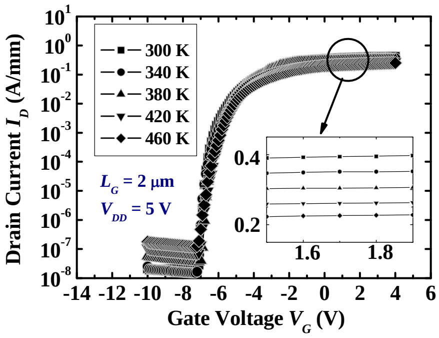

Fig. 8. I_D-V_G characteristics of AlGaN/GaN MOS-HEMT with VA and SiH_4 treatment at various temperatures (300 K, 340 K, 380K, 420 K and 460 K).

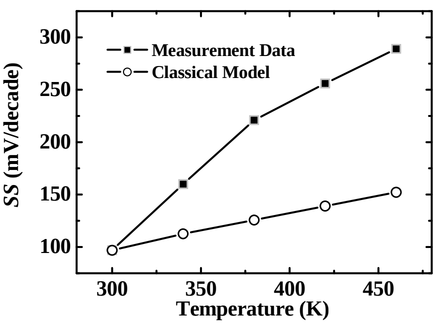

Fig. 9. Temperature dependence of *SS* characteristics of AlGaN/GaN MOS-HEMTs with VA and SiH_4 treatment at various temperatures (300 K, 340 K, 380K, 420 K and 460 K).

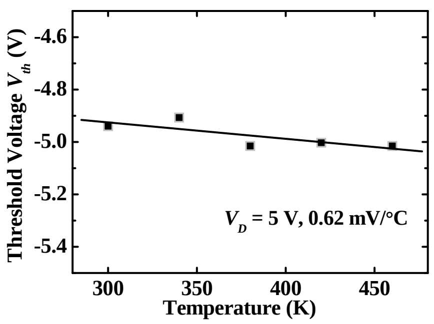

Fig. 10. Temperature dependence of V_{th} characteristics of AlGaN/GaN MOS-HEMTs with VA and SiH_4 treatment at various temperatures (300 K, 340 K, 380K, 420 K and 460 K).

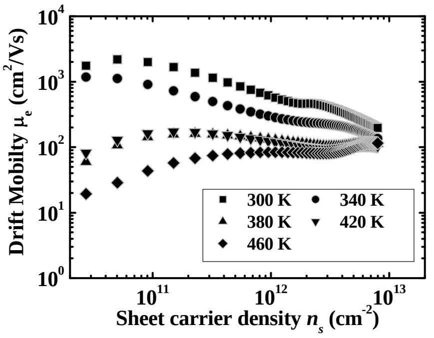

Fig. 11. Drift mobility as a function of sheet carrier density at various temperatures (300 K, 340 K, 380K, 420 K and 460 K).