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InSb MOS Diodes on a Si (111) Substrate Grown by Surface Reconstruction Controlled Epitaxy

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1. Introduction

Recently, III-V compound semiconductors have been attracted much attention as a channel material for post scaling era. Among them, InSb is one of the most promising candidates because it features highest electron mobility of 78,000 $cm^2/(Vs)$ and high saturation velocity of $5x10^7$ cm/s. High performance HEMTs based on InSb/InAlSb material system have been already demonstrated [1]. However, growth of high quality InSb on Si is difficult due to the large lattice mismatch of 19.3%. So far, most of the devices reported were grown on GaAs substrates.

Most recently, we have demonstrated that good InSb epitaxial films can be grown on Si (111) substrates using MBE via InSb bi-layer with special care to the surface reconstruction [2]. Very high mobility of 38,000 $cm^2/(Vs)$ can be obtained for relatively thin (1.2 μm) InSb on Si [3]. In this paper, we report on Al_2O_3/InSb MOS diode characteristics fabricated on InSb films grown on a Si (111) substrate using this technique.

2. Epitaxial Growth

Our growth technique is based on the finding that the InSb layer grown on a Si (111) substrate is rotated by 30 degree with respect to the substrate under a certain initial condition [2]. Figure 1 shows the schematic view of the Si atoms in a (111) surface with two InSb unit cells, non-rotated and rotated ones. As seen in the figure, 30-degree rotation drastically reduces the lattice mismatch from 19.3 % to 3.3 %. This reduction improves crystal quality of the epitaxial layers quite well.

The details of the growth procedure were reported previously [4]. Here, we describe the essence of the growth technique. A key to rotate the InSb epitaxial layer is the InSb initial bi-layer prepared by adsorption of 1 monolayer (ML) Sb onto In-induced surface reconstruction. Special care is taken here to the phase of the surface reconstruction. The InSb films were then grown by two-step growth procedure on this bi-layer. The growth temperature was 200 C for the first layer, and 440 C for the second layer, respectively.

Good quality epitaxial films (thickness 1-μm) were prepared by this growth technique. They were slightly n-type though no impurity was intentionally doped. The electron concentration and the electron mobility were estimated to be around $2x10^{16}$ cm^{-3} and 38,000 $cm^2/(Vs)$, respectively, from the data grown under the same condition.

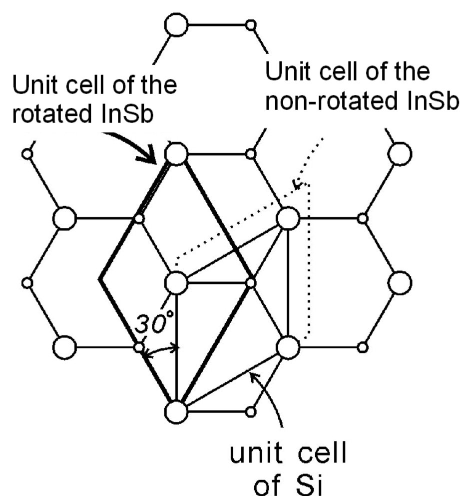

Fig. 1. Schematic view of the Si atoms in a (111) surface with rotated and non-rotated InSb unit cells.

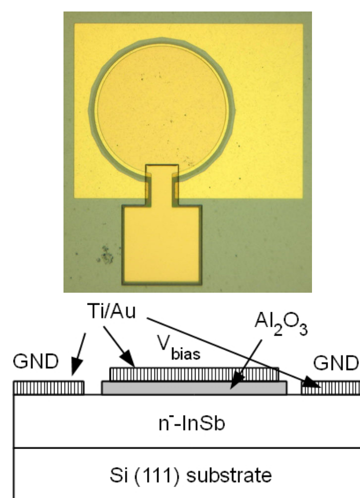

Fig. 2. Microphotograph and schematic cross-section of the fabricated Al_2O_3/InSb MOS diode.

3. Al_2O_3/InSb MOS Diode

To investigate the possibilities of InSb MOSFETs on Si substrates we fabricated Al_2O_3/InSb MOS diodes on epitaxial films grown using above technique. An Al_2O_3 insu-

lator film was deposited by using atomic layer deposition (ALD) at 250 C. Thickness of the Al_2O_3 was 30 nm. After deposition, the Al_2O_3 film was patterned by wet etching with buffered HF solution. Then, Ti/Au was evaporated and lifted off to form non-alloyed ohmic contacts and gate electrodes. The diodes were circular with diameters from 50 to 300 μm. We confirmed the capacitance of the fabricated diodes is proportional to the diode area. The structure and the microphotograph of the fabricated diode is shown in Fig. 2.

4. Capacitance-Voltage Characteristics

Figure 3 shows the capacitance-voltage curves of the fabricated diode measured at room temperature with signal frequencies of 120 Hz and 100 kHz. When the applied voltage is 2.5 V, the capacitances are close to the accumulation capacitance assuming the Al_2O_3 dielectric constant of 10. The *C-V* curves show a minimum at approximately 0V. These curves imply that the inversion occurs at negative bias together with the electron accumulation for positive bias. However, the capacitance drop at the center dip is small, only about 10 %. This is in contrast with the value expected from the Debye length, which is approximately 40%. This is probably due to the high generation-recombination rate for the narrow bandgap InSb as well as the interface states. Very similar *C-V* curves have been reported for Al_2O_3/InAs MOS diodes [5].

Then, we measured *C-V* characteristics at 77 K to investigate the effect of generation-recombination rate. The results are shown in Fig. 4. The drop at the center dip increases considerably and the *C-V* curves resemble that of conventional Si-MOS diodes. This is consistent with the ratio of thermal energy to bandgap. Anyway, these results clearly demonstrate that the interface Fermi level can be controlled by the gate voltage from the valence band to conduction band.

In our experiments, the *C-V* curves at 100 kHz still show low frequency behavior even at 77 K. We think this is due to the Ti/Au non-alloyed ohmic contact, which can work both for electrons and holes. It should be noted that the electron concentration was very low, which was close to the intrinsic carrier concentration of InSb at room temperature.

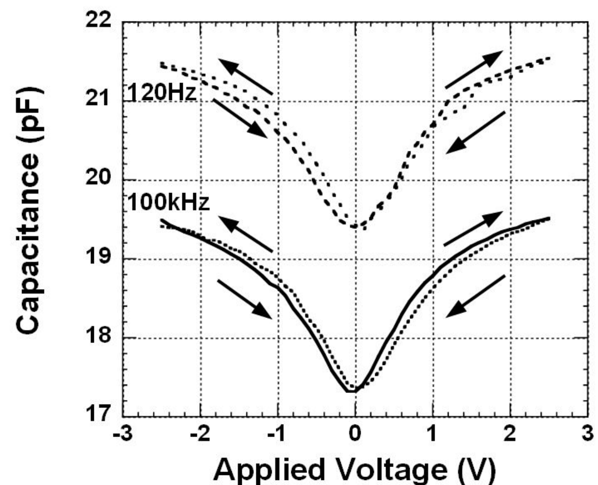

Fig. 3. Capacitance-Voltage curves of the fabricated MOS diodes measured at room temperature. The diameter of the diode is 100 μm.

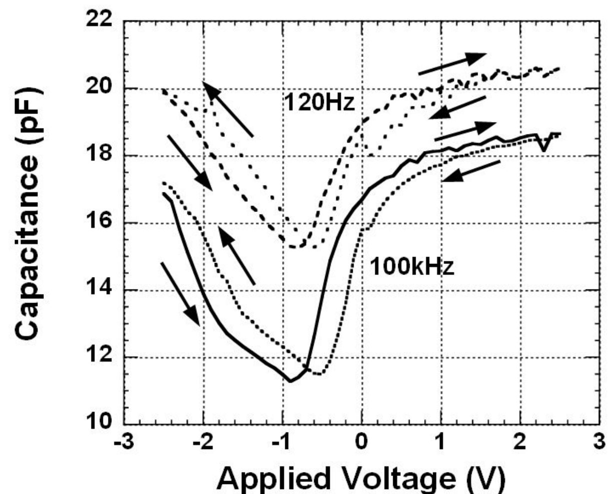

Fig. 4. Capacitance-Voltage curves of the fabricated MOS diodes measured at 77K. The diameter of the diode is 100 μm.

5. Conclusions

Al_2O_3/InSb MOS diodes were fabricated on a Si (111) substrate. Owing to the novel growth technique, good *C-V* characteristics showing inversion and accumulation were demonstrated.

Acknowledgements

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