Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp854-855

Effect of Fluorine Incorporation on $WSi_x/Al_2O_3/GaAs$ Gate Stack

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1. INTRODUCTION

III-V compound semiconductors have been considered as the alternate channel material to replace Si for the metal-oxide-semiconductor field effect transistors (MOSFETs) beyond the 22 nm technology node owing to their higher intrinsic electron mobility. However, III-V materials do not have a thermodynamically stable native oxide that can match the device performance similar to SiO_2 on Si. Several pre-gate surface passivation methods on III-V metal-oxide-semiconductor capacitor (MOSCAP) have been studied to remove the interface states [1]. However, not many post-gate treatments have been reported for GaAs MOS. Recently, fluorine incorporation into high-κ dielectric on Si [2], Ge [3] and InGaAs [4] substrates have shown improved device performance and reliability.

In this paper, we study the effect of post-gate treatment by using CF_4 plasma to incorporate fluorine (F) into the Al_2O_3 dielectric on GaAs substrate. We found out that with F incorporation, a lower dielectric constant (K_{eff}) value is obtained and the reliability of gate stack is enhanced due to fluorine passivation of interface states and bulk oxide traps.

2. DEVICE FABRICATION

The process flow for fabrication of GaAs MOSCAP is shown in Fig. 1. GaAs capacitors were fabricated on (100) p-type (~8 x 10^{17} cm^{-3}) Zn-doped GaAs and (100) n-type (~3 x 10^{16} cm^{-3}) Si-doped GaAs. Prior to an atomic layer deposition (ALD) of Al_2O_3, standard cleaning procedures were used. After these surface pre-treatments, the samples were loaded into the ALD system immediately. A layer of Al_2O_3 dielectric of about 11 nm was grown at 300 ºC using Trimethylaluminum (TMA) and H_2O as the precursors. After the Al_2O_3 deposition, some samples were treated with CF_4 plasma. WSi_x metal gate was then deposited using CVD system at 330 ºC using WF_6 and SiH_4 as the gas sources and argon as the carrier gas. Capacitors were lithographically defined and dry etched using chlorine-based reactive ion etching system. Post metallization annealing (PMA) was then performed for both CF_4 treated and control samples at 600 ºC in N_2 ambient for 30 s. A Ti/Au bilayer metal film was finally deposited using electron beam evaporator for back-contact formation.

3. RESULTS AND DISCUSSION

Fig. 2 shows the cross-sectional TEM micrographs of the GaAs MOSCAP without and with CF_4 treatment prior to WSi_x gate deposition, respectively. The thickness of Al_2O_3 is about 11 nm as shown in the inset of Fig. 2(a). This gate stack using CVD process exhibits smooth and sharp interfaces. The thickness of Al_2O_3 for MOSCAP with CF_4 treatment is similar to the control sample and the HRTEM micrograph in Fig. 2(b) also shows smooth and sharp interfaces. This proves that the CF_4 plasma does not etch Al_2O_3, which will affect the abruptness of the interfaces.

Fig. 3 shows the SIMS depth profile for the MOSCAPs with and without CF_4 treatment. The F atoms detected for the control sample are attributed to the WF_6 gas precursor used for metal gate deposition. The F concentration detected in the Al_2O_3 is higher for the CF_4 treated sample. Fig. 4 shows the *C-V* characteristics of GaAs MOSCAP with and without CF_4 plasma treatment on p and n-type GaAs. From Fig. 4(a), the CF_4 plasma treated sample shows a lower accumulation capacitance on p-type MOSCAP and hence, a lower K_{eff} due to F incorporation. The K_{eff} is 6.6 and 6.3 for the control sample and CF_4 treated sample, respectively. Though a lower K_{eff} value was obtained, F incorporation into the high-κ dielectric helps to improve the C-V characteristics of the sample, as shown in Fig. 4 where the CF_4 treated samples have lower frequency dispersion at accumulation (ΔC) and at flatband voltage (ΔV_{FB}). Fig. 4(b) shows large frequency dispersion on n-type GaAs MOSCAP as compared to p-type that could probably be due to presence of other surface imperfections such as surface kinks which generate high density of defect states in the bandgap [5]. Fig. 5 shows the distribution of interface states (D_{it}) for both p- and n-type GaAs MOSCAP measured using A.C. conductance method at 150 ºC. It is verified that the CF_4 treated samples have a lower D_{it} as compared to control samples for both p- and n-type GaAs MOSCAP. Table 1 shows the Gibbs free energy of formation of GaF_3, AsF_3 and GaAs native oxides [6]. The lower D_{it} could be attributed to energetically preferred GaF_3 and AsF_3 as compared to GaAs native oxides. These native oxides are deemed as one of the sources for interface states.

Fig. 6 shows the I_g-V_g characteristics for both the p- and n-type gate stacks. It is noticed that samples with CF_4 plasma treatment exhibit lower leakage current and higher breakdown voltage in the accumulation region as shown in Figs. 6(a) and (b). This is due to passivation of bulk oxide traps in the Al_2O_3 dielectric by the F atoms. A schematic model is proposed for F passivation as shown in Fig. 7. F atoms are able to passivate the interface states and bulk oxide traps, thereby improving the device performance of p- and n-type GaAs MOSCAP.

4. SUMMARY

F-atom incorporation into the GaAs gate stack reduces the K_{eff} of Al_2O_3 dielectric, but improves the MOSCAP characteristics by effectively passivating the interface states and bulk oxide traps, thereby improving the overall performance and reliability of the gate stack.

REFERENCES

[1] M. Houssa et al., MRS Bulletin, **34** (7), 504 (2009).
[2] C. S. Lai et al., Appl. Phys. Lett., **89**, 72904 (2006).
[3] R. Xie et al., Appl. Phys. Lett., **92**, 163505 (2008).
[4] Y. T. Chen et al., Appl. Phys. Lett., **95**, 013501 (2009).
[5] M. D. Pashley et al., Physical Review B, **48**, 4612 (1993).
[6] Yaws handbook of thermodynamic properties for hydrocarbons and chemicals

Process Flow

- Wet cleaning/passivation of GaAs surface
- ALD Al_2O_3 onto GaAs surface
- CF_4 plasma treatment
- WSi_x metal gate deposition and patterning
- PMA
- Ti/Au back contact formation

Fig. 1. Process flow used for fabrication of p- and n-GaAs MOSCAP.

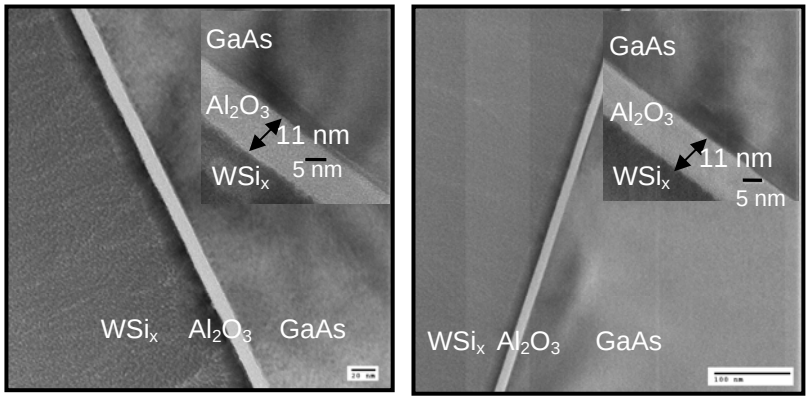

Fig. 2. Cross-sectional TEM micrographs of the gate stack of (a) control sample and (b) CF_4 treated sample and their corresponding HRTEM micrographs in the inset. The oxide thickness and interface roughness for (a) and (b) are similar implying that the CF_4 plasma does not etch Al_2O_3.

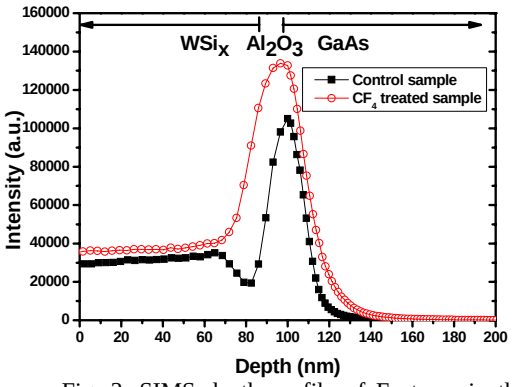

Fig. 3. SIMS depth profile of F atoms in the $WSi_x/Al_2O_3/GaAs$ gate stack for samples with and without CF_4 plasma treatment.

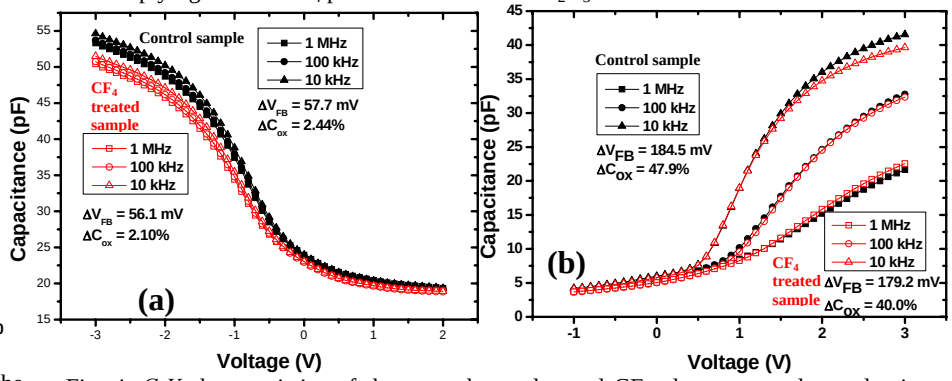

Fig. 4. *C-V* characteristics of the control samples and CF_4 plasma treated samples in a range of 10 kHz to 1 MHz frequencies on (a) p-type and (b) n-type GaAs MOSCAP.

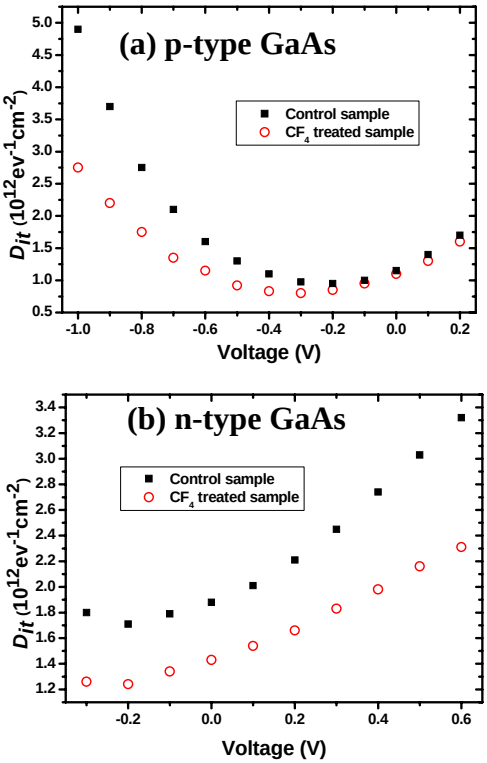

Fig. 5. Plots of D_{it} vs gate voltage for control samples and CF_4 plasma treated samples on (a) p-type and (b) n-type GaAs MOSCAP.

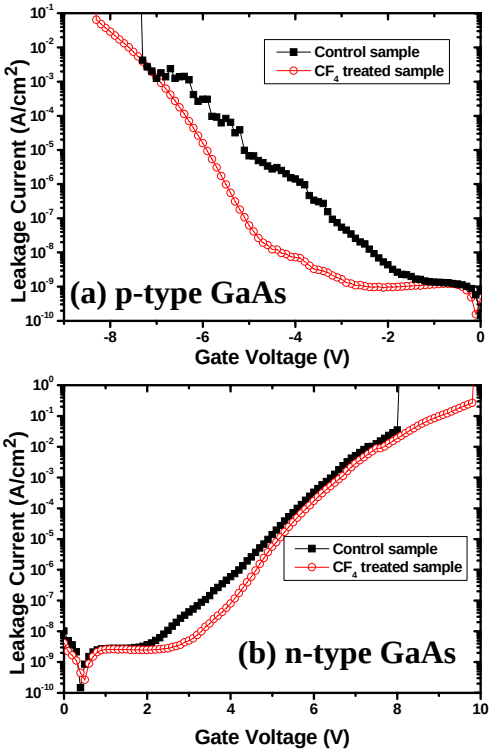

Fig. 6. Gate leakage (I_g-V_g) characteristics for control samples and CF_4 plasma treated samples on (a) p-type and (b) n-type GaAs MOSCAP.

Table 1. Gibbs free energy of formation for Ga and As oxide and fluoride [6].

	Gibbs free energy of formation, ΔG_f(kJ mol^{-1})	
Ga	Ga_2O_3	-998
	GaF_3	-1085
As	As_2O_3	-569
	AsF_3	-771

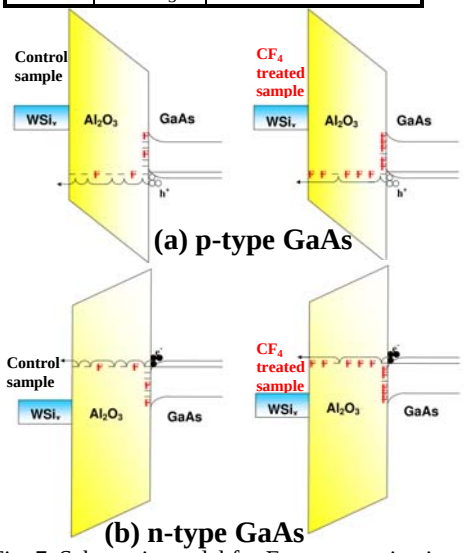

Fig. 7. Schematic model for F atoms passivation of interface states and bulk oxide traps for (a) p-type and (b) n-type GaAs MOSCAP in accumulation region.