Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp862-863

Recombination Model at Perimeter of Stacking Faults in 4H-SiC pin Diode with Forward Voltage Drift

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1. Introduction

SiC possesses excellent electrical and physical properties and some high-voltage SiC bipolar devices offering performance have been developed. However, these SiC bipolar devices possess serious problems. One of them is a forward voltage (V_F) drift problem, which is an increase in V_F drop during forward bias operation, due to expanded stacking faults (SFs) in the drift layer [1]. V_F drift results in increased electric power loss and subsequently higher temperatures for SiC bipolar devices, culminating in device destruction. Some epitaxial growth techniques have recently been developed in order to reduce SFs and thereby curtail V_F drift [2,3]. However, an ideal reduction is difficult [4]. Therefore, it is highly significant to investigate the V_F drift effect on the electrical characteristics. We reported the relation between the forward and the reverse recovery characteristics [5], but the mechanism has not been clarified yet.

In this paper, we investigated the relation between the forward and the reverse recovery characteristics of the pin diode with the V_F drift. Moreover, we propose the recombination model at the perimeter of the SFs.

2. Experimental Methods

2-1. Device Fabrication

Fig. 1 shows the device structure of the fabricated 4H-SiC pin diode with mesa-JTE (Junction Termination Extension). The drift layers were formed by epitaxial growth on the n-type 4H-SiC Si-face substrates off-angled by 8° toward <11-20>.

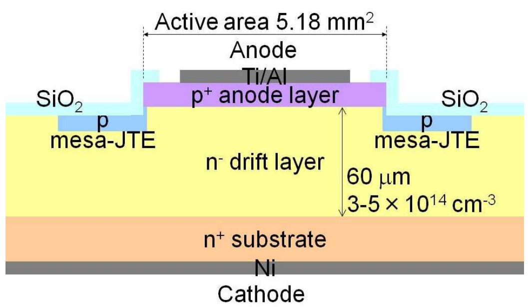


Fig. 1. Device structure of fabricated 4H-SiC pin diode with mesa-JTE.

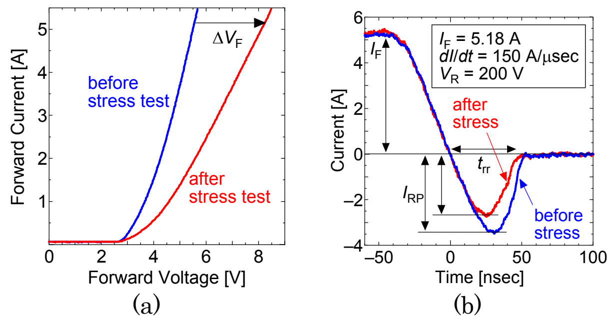


Fig. 2. Typical (a) forward and (b) reverse recovery characteristics of fabricated pin Diode before and after stress.

2.2 Forward Characteristics of Fabricated pin Diode

The stress was conducted at 100 A/cm^2 for one hour. Fig. 2 (a) shows the typical forward characteristics of the fabricated pin diodes. The symbol ΔV_F represents the V_F difference at 100 A/cm^2 and at room temperature between before and after the stress.

2.3 Reverse Recovery Characteristics of Fabricated pin Diode

Fig. 2 (b) shows the typical reverse recovery characteristics of the fabricated pin diodes. The recovered charge (Q_{rr}) and the hole lifetime (τ_p) can be given by [6],

$$Q_{rr} = \frac{1}{2} I_{RP} t_{rr}, \ \tau_p = 2 \frac{I_{RP}}{I_F} t_{rr}, \qquad (1)$$

where I_{RP} is the peak reverse recovery current, t_{rr} is the reverse recovery time and I_F is the conducting current under forward bias. The symbol $\Delta\tau_p$ represents the τ_p absolute difference between before and after the stress.

3. Results and Discussions

3.1 Forward and Reverse Recovery Characteristics

Fig. 3 shows the dependence of $\Delta\tau_p$ on ΔV_F of the fabricated pin diodes. $\Delta\tau_p$ increases with an increase in ΔV_F. The solid lines show the relations calculated by using the method in the next section.

The V_F drift is caused by an expansion of the SFs created by the penetration of basal plane dislocations (BPDs) into the drift layer. The SFs in the drift layer of the pin diode with V_F drift reduce the carrier lifetime, and the SFs create barriers for the flow of current in the drift layer of the pin diode [1]. The current flow areas in the device are remarkably narrowed by expansion of the SFs, and V_F increases. On the other hand, τ_p does not depend on a current flow area from Equation (1). Nevertheless, the pin diodes with V_F drift have fast turn-off characteristics as compared with these before the stress.

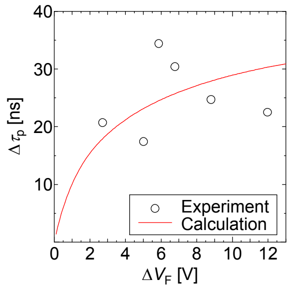


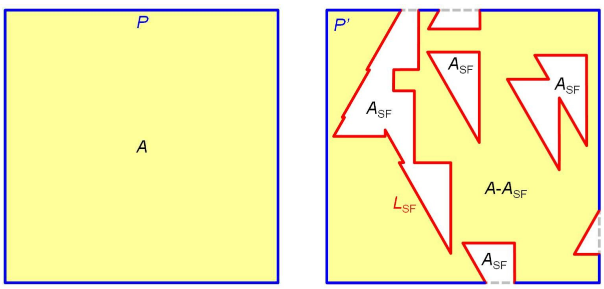
Fig. 3. Dependence of $\Delta\tau_p$ on ΔV_F of fabricated pin diodes.

3.2 Recombination at Perimeter of SFs

As recombination occurs at the perimeter and the bulk of the pin diode, the minority carrier lifetime (τ_0) calculated from reverse recovery characteristics can be given by [7],

$$\frac{A}{\tau_0} = \frac{A}{\tau_{\mathrm{bulk}}} + s_P P, \tag{2}$$

where τ_{bulk} is the intrinsic hole lifetime determined by bulk recombination, s_P is the surface recombination velocity at the perimeter of the pin diode, A and P are the area and the perimeter of the pin diode, respectively, as shown in Fig. 4 (a).



(a) (b)

Fig. 4. Typical distribution images of SFs in drift layer (a) before and (b) after stress.

τ_p of the pin diode with V_F drift becomes small as compared with that before the stress, therefore we assumed that the recombination at the perimeter of the SFs could not be ignored. Under assumption of the recombination at the perimeter of the SFs, the minority carrier lifetime (τ_1) of the pin diode with V_F drift can be given by,

$$\frac{A - A_{\mathrm{SF}}}{\tau_1} = \frac{A - A_{\mathrm{SF}}}{\tau_{\mathrm{bulk}}} + s_P P' + s_{\mathrm{SF}} L_{\mathrm{SF}}, \tag{3}$$

where P' is the effective perimeter of the pin diode without existing the SFs, s_{SF} is the surface recombination velocity at the perimeter of the SFs, A_{SF} and L_{SF} are the total amount of area and the perimeter of the SFs, respectively, as shown in Fig. 4 (b).

By using Equation (2) and Equation (3), it can be shown that,

$$\alpha = \frac{1}{\tau_{\mathrm{bulk}}}\beta - s_{\mathrm{SF}}, \tag{4}$$

where,

$$\alpha = \frac{A_{\mathrm{SF}}}{L_{\mathrm{SF}}}\left[\frac{A_{\mathrm{SF}}}{A}\left(\frac{1}{\tau_0}\frac{P'}{P} - \frac{1}{\tau_1}\right) + \frac{1}{\tau_1}\right], \tag{5}$$

$$\beta = \frac{A_{\mathrm{SF}}}{L_{\mathrm{SF}}}\left[1 + \frac{A_{\mathrm{SF}}}{A}\left(\frac{P'}{P} - 1\right)\right]. \tag{6}$$

Overlaps of the SFs could not be ignored in the actual devices, therefore α and β calculated from τ_0, τ_1 and ΔV_F by using Monte-Carlo Method. Fig. 5 shows the dependence of α on β of the fabricated pin diodes. The clear dependence revealed that the τ_p shortened by the recombination at the perimeter of the SFs.

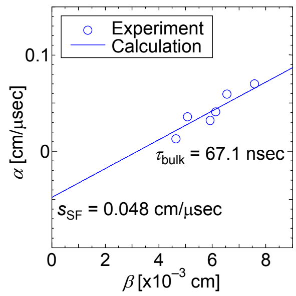


Fig. 5. Dependence of α on β of fabricated pin diodes.

4. Conclusions

The recombination model at the perimeter of the SFs was proposed. It was revealed that the τ_p shortened by the recombination at the perimeter of the SFs.

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