Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp874-875

Novel Passivation Layer for Improvement of Reliability In Amorphous Indium Gallium Zinc Oxide Thin Film Transistors (TFTs)

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1. Introduction

Recently, amorphous oxide semiconductors (AOSs) thin-film transistors (TFTs) required for high resolution display such as active matrix organic light emitting diode (AMOLED) due to its high current driving ability as the resolution of display increases compared to amorphous silicon, which is the present-day dominant TFT technology for large-area application [1].

One of the most widely used AOS materials is indium-gallium-zinc-oxide (IGZO), as already proposed by Hosono et al. of the Tokyo Institute of Technology in 2004 [2]. However, the reliability of oxide TFTs is critical issue under electrical bias stress with light illumination [1]. Passivation method of a-IGZO TFTs is also important for maintaining the electrical properties of devices in terms of applying into integrated circuit applications [3].

The purpose of our work is to improve the reliability of a-IGZO TFTs on the glass substrate by employing the novel passivation layer. Proposed passivation layer consisting of 2-step deposition grown at different substrate temperatures. Proposed passivation method makes devices with reliable electrical characteristics against electrical bias stress - light illumination condition.

2. Device Fabrication

We have fabricated inverted-staggered bottom-gate TFTs on the quartz-glass substrates as shown in Fig. 1. At first, a 100nm thick chromium (Cr) gate electrode was deposited by e-beam evaporation and gate oxide (SiO_2, 320 nm thick) was deposited. Then, a-InGaZnO thin-films (60nm) were deposited in an Ar/O_2 gas mixture at room temperature using by an RF magnetron sputter. RF magnetron sputtering was performed using an RF power of 360W in 2mTorr. The ceramic, which is 4-inch In_2O_3: Ga_2O_3: ZnO = 1:1:1 (LTS, Inc.), was used during deposition.

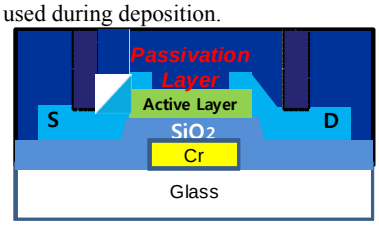

Fig. 1 Cross Section view of fabricated a-IGZO TFT on the quartz-glass substrate.

A 300nm thick indium-tin oxide (ITO) source/drain electrode layer was deposited by DC magnetron sputtering. Film definition was accomplished using photo masks, resulting in a channel length / width of 20μm /100μm.

After forming the source/drain electrodes, the backside of the channel layer was passivated by 300nm thick SiO_2 passivation layer. Passivation layer and gate insulator procedures were carried out in an inductively coupled plasma-chemical vapor deposition (ICP-CVD) system, respectively.

3. Results and Discussion

For the passivation layer, three kinds of SiO_2 film were deposited by ICP-CVD as shown in Fig. 2. First one (I) is a 300nm thick SiO_2 was formed at 150°C which is low enough to maintain the electrical characteristics of a-IGZO semiconducting thin film during deposition. Compared with one deposited at higher temperatures, the solidity of that film exhibits less dense. Second one (II) is a 300nm thick SiO_2 was formed at 300°C which is high enough to protect the environmental effects. Yet, it could damage on the active layer by accelerating the decomposition of radicals in ICP-CVD chamber during deposition process.

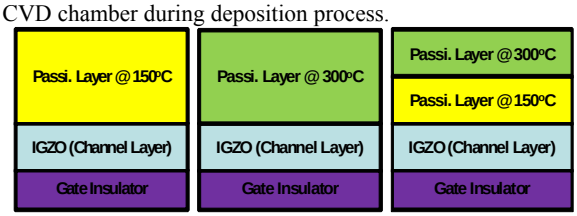

Fig. 2 a-IGZO TFT with (a) single-passivation layer (I) (150°C deposited (300nm)), (b) single-passivation layer (II) (300°C deposited (300nm)), and (c) dual-passivation layer (III) (150°C deposited (150nm) / 300°C deposited (150nm)) on the quartz-glass substrate.

To solve these problems, the novel passivation layer was proposed. That is, last one (III) is dual-passivation layer which is made of a 150nm thick ICP-CVD SiO_2 layer deposited at 300ºC on top of an initial 150nm thick SiO_2 layer grown at 150ºC. The underlying low temperature (150ºC) deposited SiO_2 layer is firstly deposited in order to prevent the a-IGZO active layer by hydrogen (H) incorporation, which is the cause of making the a-IGZO thin film conductive [4].

An agilent B1500A semiconductor parameter analyzer is used to monitor all electrical characteristics in the dark condition. Before the measurements, the a-IGZO thin-films were annealed at 623K for 1hours (on air). The saturation mobility of the single-passivation layer (I), (II) TFTs was 15.1 cm^2/Vs and 12.6 cm^2/Vs. And the saturation mobility of the dual-passivation layer TFT is 24.1 cm^2/Vs. It is evident that the proposed device exhibits the higher saturation mobility.

In order to find the effectiveness of dual-passivation layer in oxide TFTs under operation circumstances, we have applied a fixed gate and drain bias V_{GS}= -20V, V_{DS} = 0V on the a-

IGZO TFT with 5mW/cm^2 light illumination (Halogen lamp) to oxide TFT for 5,000 seconds (NBIS: Negative Bias Illumination Stress).

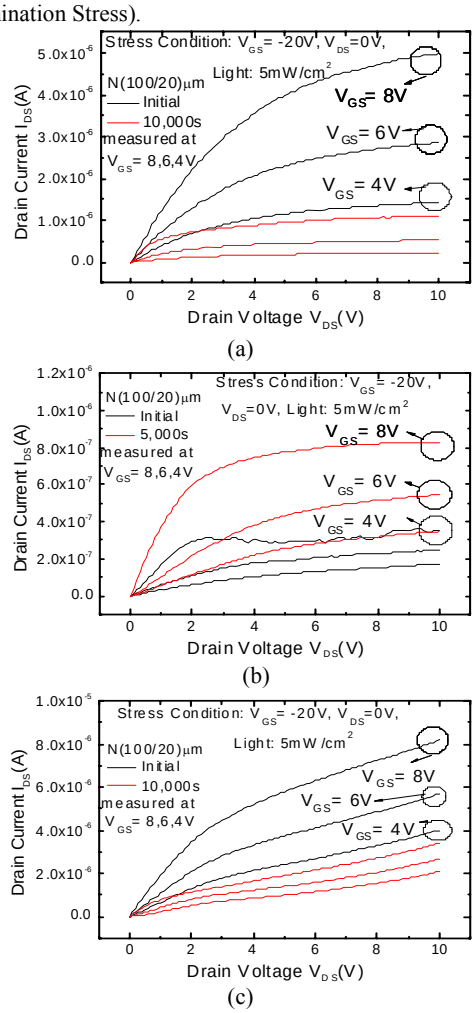

Fig. 3 Output characteristic of a-IGZO TFT with (a) single-passivation layer (I), (b) single-passivation layer (II), and (c) dual-passivation layer (III) before and after negative gate bias stress time (V_{GS} = -20V, V_{DS}= 0V, 5000s) with 5mW/cm^2 light illumination.

After the NBIS, at V_{DS}= 10V and V_{GS}= 8V, 58.1% reduction of drain current of a-IGZO TFT with stress time was occurred in the a-IGZO TFTs with dual-passivation layer (III) compared to unstressed device, whereas the single-passivation layer (I) / (II) exhibits a 77.7% and -135% reduction of output current, as shown in Fig. 3.

Furthermore, we also evaluated the electrical stability of TFTs with dual-passivation under V_{GS}= 20V, V_{DS} = 0V on the a-IGZO TFT with 5mW/cm^2 light illumination (Halogen lamp) for 5,000 seconds (PBITS: Positive Bias Illumination Temperature Stress). After the PBIS, at V_{DS}= 10V and V_{GS}= 8V, 173% increase of drain current was occurred in the a-IGZO TFTs with dual-passivation layer (III) compared to unstressed device, whereas the single-passivation layer (I) / (II) exhibits a 360% and 292% increase of output current as shown in Fig. 4.

Drain current of proposed device was not changed so much compared with that that of TFTs with single-passivation layer (I), (II). Proposed device exhibits less degradation, indicating that appropriate dual-passivation method leads to better bias-illumination reliability.

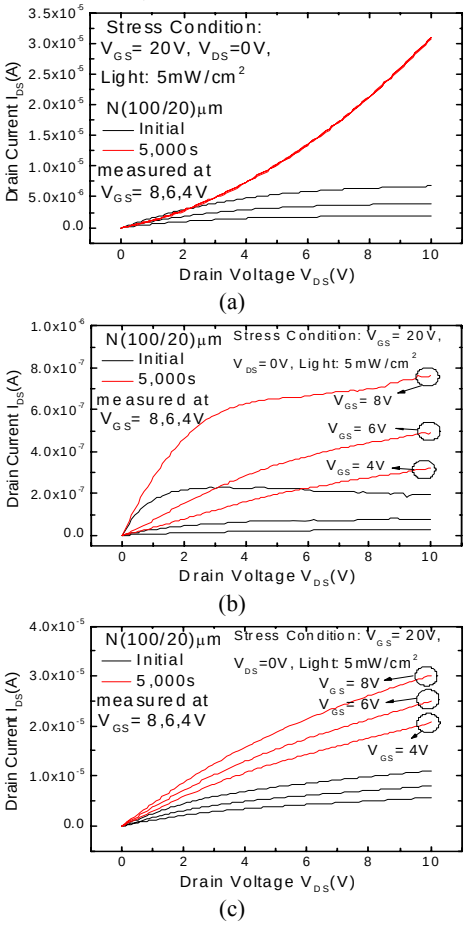

Fig. 4 Output characteristic of a-IGZO TFT with (a) single-passivation layer (I), (b) single-passivation layer (II), and (c) dual-passivation layer (III) before and after positive gate bias stress time (V_{GS} = +20V, V_{DS}= 0V, 5000s) with 5mW/cm^2 light illumination.

Because the fabrication processes were totally same except the passivation process, it could be verify that proposed dual-passivation method is suitable for improving the reliability of the a-IGZO TFTs without any additional process.

4. Conclusion

We have proposed and fabricated the a-IGZO TFTs with novel passivation layer consisting of sub-layers with different substrate temperatures. And we have verified that the proposed device could improve bias-illumination stability and enhance the electrical characteristics of a-IGZO TFTs.

5. References

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