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GaN on Si Based Power Devices : A New Era in Power Electronics

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1. Introduction

Since the advent of the spontaneous AlGaN-GaN based high electron mobility sheet formation, first discovered by M. Asif Kahn in 1991 [1], significant efforts have been made to bring the inherent capabilities of this exciting material system to bear in practical semiconductor power devices. The combination of high breakdown field strength due to the wide band gap of the III-nitrides and the high electron mobility provided by the 2 DEG at the hetero-junction, as well as an unusually high electron density yield a remarkably compelling drift resistance, particularly for operating voltages in excess of 150 V. Such devices also benefit from the reduced gate charge requirements involved in switching the devices on and off, especially important for high frequency application, typically with voltages < 100 V. Probably the most exciting attribute of the system involves the easily isolating nature of the inherently lateral devices, permitting unprecedented monolithic integration of power systems. From a technologist's point of view, it is unfortunate that, as in many such inherently superior technological alternatives, economics more than physics will determine the rate and extent of adoption of GaN based power devices.

2. The Driving Metric

The driving metric for adoption of new semiconductor technologies is performance/cost (P/C). This is the same as used in the popular Moore's Law for data processing technology. It is therefore imperative that focus be placed not on performance alone but at least equally on the fundamental factors that drive the economics of the technological proposition.

In the case of GaN based power devices, one of the single greatest factors affecting cost is the choice of substrate material. As the adoption of any new device structure must compete with that of the incumbent, the vast majority currently being silicon based devices, the cost of substrate and epitaxial growth should not far exceed the cost for a comparable fully fabricated silicon device. If one considers that the advantage in P/C of the new device should be at least 2-3 times that of the incumbent, and a projected 4 to 10 times improvement in performance, then a factor of 2-3 higher in cost would be a reasonable upper target. This sets an upper limit of about $ 3/cm2 for the combined cost of substrate and epitaxial layer. Only silicon substrates meet this requirement. The use of silicon substrates for GaN hetero-epitaxy present several significant technical challenges due to large mis-matches in thermal coefficient of expansion as well as lattice constants of the materials. In addition, device fabrication processing costs must be competitive with CMOS based silicon processing often performed in large scale foundries processing > 20,000 wafers per week. Therefore, in order to achieve the required performance/cost, GaN based devices should be processed in the same high volume foundries, using as much of the same high throughput, high yielding process technologies as used for silicon based devices as possible. Today, this requires that the substrates be at least 150 mm, preferably 200 mm, in diameter, further exacerbating the consequences of material property mismatch.

Device performance requirements are not limited to such figures of merit as on-resistance or gate charge. Leakage currents, for instance, should achieve the performance levels of incumbent silicon devices. This is to say that the criteria for both breakdown voltage and leakage currents (gate and source-drain) must be adjusted down from that commonly used when discussing GaN based devices of mA/mm of gate periphery to a more practical 0.1 to 1 uA/mm. In addition, device quality, stability and reliability are all to be considered first order requirements for successful commercialization of any new technology, with the incumbent silicon platform setting the standard.

3. A Commercially Viable Platform

A technological platform that meets the performance and cost requirements described above has been developed by International Rectifier, referred to as GaNpowIR. This platform uses multi-wafer MOCVD reactors to grow GaN epitaxy on standard thickness (675 µm) 150 mm silicon substrates. Wafer bow for 2 µm of epitaxial films is routinely less than 20 µm. The device processing is fully compatible with silicon CMOS foundries and is based on thin film photo and etch lithography. The ohmic contacts are formed without the use of gold metallurgy and provide a contact resistance of 0.25 +/- 0.1 mohm mm including cross wafer, wafer to wafer and lot to lot variations. The two dimensional electron gas formed at the interface between the AlGaN barrier and GaN channel layers routinely provides carrier mobility of greater than 2000 cm^2/Vs. Threading dislocations which intercept the AlGaN surface are approximately $1\ 10^9\ cm^{-2}$. Fabricated low voltage devices routinely exhibit Ion/Ioff ratios of $> 10^{12}$ for Vdrain

of 12 V and Vg = -7 V, with leakage currents less than 0.1 pA/mm. In fact high voltage devices have been routinely shown to exhibit Ion/Ioff ratios in excess of 10^7, where Ioff is measured at 600 V at less than 0.1 uA/mm for Vg=-10 V. In addition, the use of an insulated gate provides gate leakage currents of less than 0.1 pA/mm.

4. First Products

The first product family introduced on the GaNpowIR platform are intended to service low voltage dc-dc point of load applications, namely 12 Vin to 0.6 to 3.3 Vout. With gate lengths of 0.3 µm, gate widths of 1 to 3 meters, source drain distance of 2.3 µm and a gate-drain spacing of 1 um, the devices exhibited a punchthrough limited source-drain breakdown voltage in excess of 30 V with Vg= -10 V. The low voltage GaN based devices exhibit a typical performance of 30 mohm-nC for gate charge times Rdson(AA) figure of merit. This is significantly better than state of the art silicon based devices. The resulting power conversion efficiency for the point of load converters at 600 kHz is 3 to 4 % better than competing solutions based on silicon devices. As discussed elsewhere [2] the potential for this technology is to achieve an R-Qg figure of merit <5 mOhm-nC with corresponding improvements in power conversion efficiency.

5. Device Ruggedness

It is imperative that any new device technology be demonstrated as robust as the incumbent silicon based solutions. In Figure 1, the long term stability of the device gate leakage under extreme bias conditions (-50 V at 150 C) is shown over 3000 hrs. Figure 2 shows that the device Rdson is also very stable for over 6000 hrs under high temperature reverse bias stress. To date, over 3 million device hours under accelerated conditions have demonstrated stable parametric behavior for these low voltage GaN based devices.

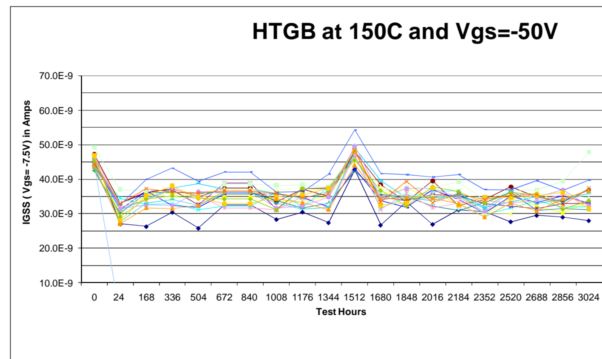

Figure 1: Stability of gate leakage current over 3000 hrs with -50 V applied to the 8.5 V rated gates at 150 °C.

The measured forward biased safe operating area (FBSOA) for these low voltage devices is shown in Figure 3. As can be seen, the FBSOA is significantly greater than that required by the 12 Vin application. Further, it has been found that the FBSOA is essentially independent

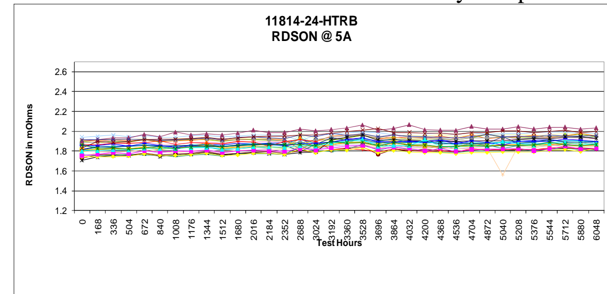

Figure 2: Stability of on-resistance, Rdson for low voltage GaN based power devices at 150 C, with Vg=-7V and Vds= 15 V over 6000 hrs.

of ambient temperature to greater than 125 C, when packaged in a standard SO-8.

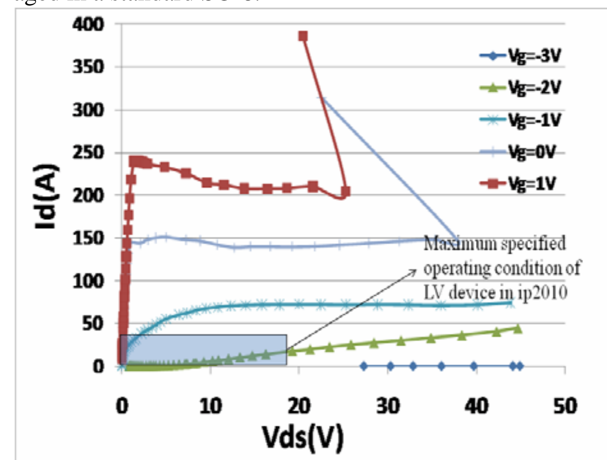

Figure 3: Forward biased SOA for low voltage GaN based power devices intended for 12Vin power conversion applications.

To the author's knowledge, these results represent the first commercially viable application of GaN based power conversion devices and herald a new era in power electronics through the combination of high performance and competitive costs for semiconductor power devices.

3. Conclusions

A first example of commercial viability for GaN on Si based power devices is presented, showing significantly enhanced performance, as well as a competitive cost structure. Excellent long term stability of parametric performance such as Rdson and gate leakage current have been demonstrated to over 6000 hrs. In addition, excellent forward biased safe operating area for these low voltage devices has been demonstrated.

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References

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[2] Briere, M.A., Power Electronics Europe **7**, (2008) 29