Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp1229-1230

Direct Liquid Cooling Technology for Power Semiconductor Devices

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1. Introduction

Novel power devices such as GaN and SiC transistors are widely investigated for high power and high voltage switching applications taking advantage of their superior material properties. Tremendous reductions of chip size are realized due to its low on resistance. Power concentration in a small chip requires superior thermal distribution properties to eliminate thermal limitation of device performances. Compound semiconductor devices on silicon or sapphire substrate have remained low thermal conductivity of the substrate. Direct heat transfer from a chip surface is expected as well as conventional heat transfer through the substrate.

Direct liquid cooling (DLC) of a transistor surface is one candidate to realize thermal elimination from a chip surface maintaining electrical isolation. Increase in thermal conductivity due to latent heat of vaporization from the chip surface is demonstrated in a package based on a heat pipe structure. Comparison of a heat pipe with a solid metallic conductor of the same cross section shows that a heat pipe can transport as much as a thousand times more energy for the same temperature difference [1,2]. DLC has advantages as extremely high values of thermal conductance, electrical isolation while retaining high thermal conductance, widely varying thermal fluxes without variation in temperature, and reduction of local temperature variation or hot spotting

This paper describes advanced thermal management techniques to reduce operating junction temperatures in direct liquid cooling of GaN power devices for the first time.

2. Experiments

Device structure

A normally-off AlGaN/GaN gate injection transistor (GIT) was mounted in a direct liquid cooling (DLC) package. The heterojunction field effect transistor features p-AlGaN gate over AlGaN/GaN hetero-structure to serve the normally-off operation. High drain current with low on-state resistance can be achieved in the GIT taking advantages of so-called conductivity modulation by hole injection from the p-type gate [3-6]. Gate width of GIT was 100mm and chip size was 3mm×3mm.

Structure of Direct liquid cooling package

The DLC package constructed of a container part and a stem part is shown in Figure 1. A GIT chip was eutectically bonded by Au-Sn solder or mounted by silver paste technique on a TO-type stem. Although Au-Sn solder is suitable for low thermal resistance, silver paste has the advantage of small mechanical stress in a semiconductor chip due to its low degree of hardness.

The stem is made of cold rolled steel (SPCE) for achieving hermetical seal to glue up electrodes. Stem periphery is wrapped by cupper ring for the sake of laser welding to the cupper container. In the package, ethanol was selected as a suitable volatile working fluid. Ethanol has poor merit number rather than water, but ethanol is suitable for its insulation properties and superior corrosion-resistance to GaN related materials. No gas other than the pure vapor of the fluid is present. The DLC package consists of a sealed Cu container with a wick which is wet with the working fluid. The size of container was 15mm in diameter and 100mm long.

The DLC package is defined as a device that transfers heat by evaporation on liquid from heated areas and condensation on cold areas, with continuous return of the condensate to the heated area by capillary action. The temperature along the wick surface will then be essentially constant at the equilibrium temperature for the liquid-vapor interface at the given pressure. The primary thermal resistance of DLC package is usually caused by the conduction of heat through the container wall and wick structure.

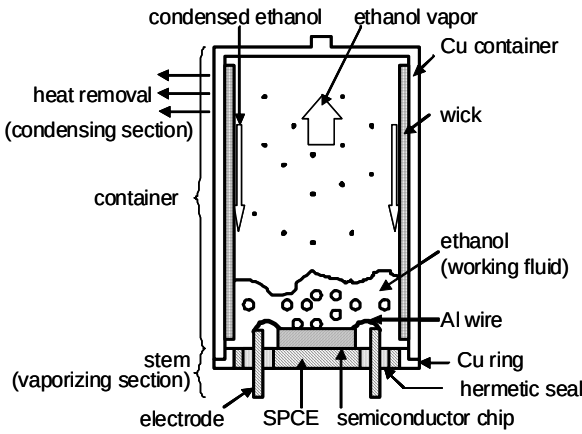

Figure 1. Schematic of DLC Package. The package is a sealed enclosure. The inside is wetted with a suitable volatile dielectric working fluid.

Measurement of thermal resistance

Thermal resistance (R_{th}) is a measure of the amount by

which the junction temperature rises from ambient air temperature (ΔT_j) for a given level of power dissipation (P_D) in a transistor. Thermal resistance is important since it determines how much power a device and package combination can safely dissipate. Therefore, thermal resistance is an important figure of merit for how well a transistor package and heat-sink combination is able to dissipate heat and thus to what power level the device may safely be run.

To measure thermal resistance ($R_{th}=\Delta T_j / P_D$), the two variables to be measured are P_D and ΔT_j. Power dissipation is simply obtained from the voltage drop (V_D) across the transistor and the current (I_D) through it adding a drain-source current pulse (pulse width: t_D), as $P_D= I_D \times V_D$. Junction temperature is characterized by a technique called K-factor calibration ($K=\Delta T_M / \Delta V_M$) in which a gate-source voltage (V_M) and ambient temperature (T_M) dependency of the transistor is first characterized where a small measurement current level (I_M=2mA) to bias above the cut-in voltage is used. Junction temperature rise (ΔT_j) between before and after power dispersion is calculated from gate-source voltage change (ΔV_M) using K-factor ($\Delta T_j=\Delta V_M \times K$).

3. Results and discussions

Junction temperature characteristics were measured for GITs with or without working fluid. The measurements of this study were carried out in an ambient condition without radiator. The dependence of junction temperature rise on power dissipation was studied varying in I_D from 0.2 to 2A (V_D = 10V, t_D= 0.1s).

Figure 2 demonstrates reductions in junction temperatures of up to 55K or 100 percent higher power levels with the same ΔT_j with the application of DLC.

Transient thermal resistance characteristics of DLC are shown in Figure 3. Thermal resistance was measured varying in t_D from 100μs to 100s (I_D=10A, V_D=10V). In the case without DLC (solid square) in which ethanol was not filled in the container, the thermal resistance increased with t_D of more than 9.5K/W for 30s power dissipation.

The DLC packages mounted by Au-Sn solder (open square) or silver paste (open diamond) represent the decrease in the thermal resistance.

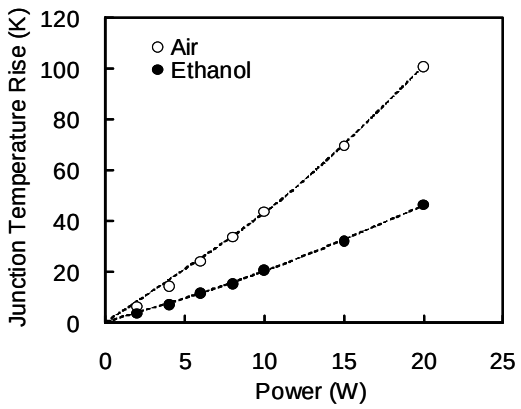

Figure 2. GIT junction temperature rise. Junction temperatures are compared for transistors with (closed circle) or without (open circle) DLC.

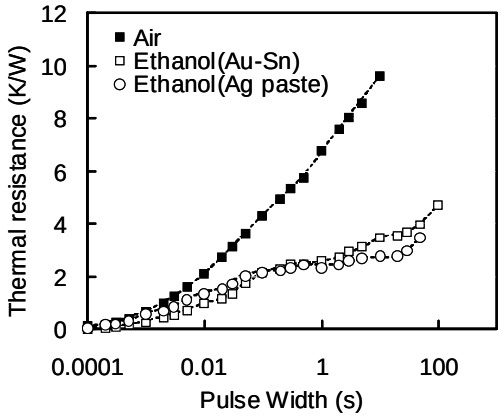

Figure 3. GIT transient thermal resistance characteristics. Drastic reduction of thermal resistance is realized in DLC (open square: Au-Sn solder, open circle: silver paste).

For silver paste case, the thermal resistance was less than 3K/W in an ambient condition without radiator. The thermal resistance from junction to ambient for a GIT has been reduced as much as 32 percent by incorporating the DLC structure inside the package.

In this study, the measurement took place in ambient condition without radiator. Superior reduction of thermal resistance is expected in the forced-air-cooled conditions.

4. Conclusions

We first demonstrate the reduction of junction temperatures in direct liquid cooling of GaN power devices for high power and high voltage switching applications. In the package, ethanol is filled as a volatile working fluid. Junction temperature reductions of up to 55K or 100 percent higher power levels were demonstrated with the application of DLC. The thermal resistance has been reduced as much as 32 percent in the DLC structure. DLC has advantages as excellent thermal conductor in that it utilizes nonmetallic, nonelectrically conductive materials in order to maintain electrical isolation for high power and high voltage devices while retaining high thermal conductance.

Acknowledgements

The authors would like to gratefully acknowledge Dr. T. Tanaka and Dr. T. Ueda for the technical advices on the GIT devices.

This work is partially supported by the New Energy and Industrial Technology Development Organization (NEDO), Japan, under the Strategic Development of Energy Conservation Technology Project.

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