

New Stacked MIM Capacitors with Side-contact Formation Technology

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1. Introduction

InP ICs for future 100-Gbps optical transport networks have been improved, recently^{[1],[2]}. However, it is still necessary to make the IC chips smaller in order to reduce electrical loss and chip cost or to boost the resonance frequency outside of the operation range. For making IC chips smaller, increasing the capacitance density ($\text{fF}/\mu\text{m}^2$) would be very effective because capacitors occupy a large area of IC chips.

Stacking MIM capacitors is a very promising way to increase capacitance density for InP-based ICs, but the conventional stacked MIM capacitor structure requires many masks for multilayer-MIM electrodes and the fabrication process is complicated^{[3],[4]}.

In this study, we proposed a new stacked MIM capacitor structure in which each electrode is connected with electrical side-contacts, which enables fabrication with very few masks and a short turn-around time. We successfully fabricated a five-layer stacked MIM capacitor and increased capacitance density by a factor of 5, from $0.30 \text{ fF}/\mu\text{m}^2$ to $1.51 \text{ fF}/\mu\text{m}^2$.

2. Experiment

As shown in Fig. 1, the multilayer structure consists of two kinds of MIM electrodes and dielectrics. The electrodes are made by using photolithography masks, which are used alternately and repeatedly. One type of electrode has two or more small holes in it, and the other type has two or more large holes in the same places as the small holes. After the multilayer structure has been formed, vias connecting the layers are formed in one step. This technique enables MIM capacitors with high-capacitance density to be fabricated with very few masks and a short turn-around time.

Figure 1(a) shows how the stack structure is formed. After the SiO_2 layer (200 nm) is deposited on a substrate, a single-layer MIM capacitor is formed by lift-off techniques for the electrodes and by plasma-enhanced chemical-vapor deposition (PECVD) for the dielectric layer. Then, SiN layers for use as a dielectric and the two-types of electrodes A and B are formed, followed by the deposition of a 300-nm-thick SiN passivation layer on top of the MIM structures. Next, through-holes for connecting all of the electrodes are formed by SF_6 reactive-ion etching (RIE) in one step as shown in Fig. 1(b). Then, over-etching is performed to side-etch (0.3- μm target) the through-holes in preparation for the formation of electrical side-contacts

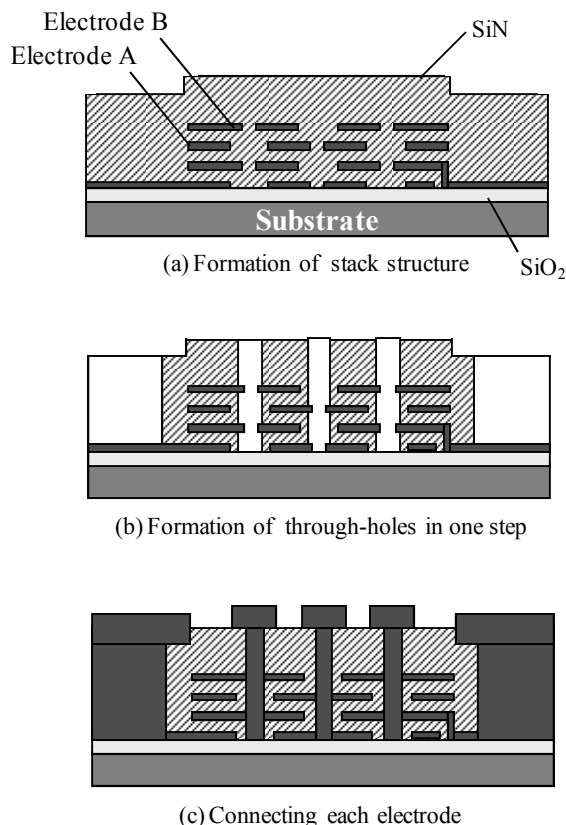
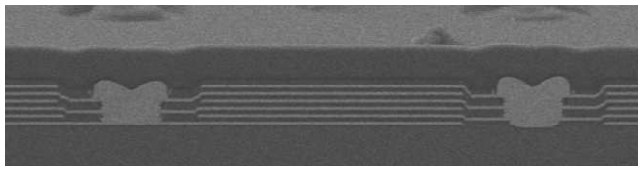


Fig. 1. Fabrication of stack type MIM capacitor.

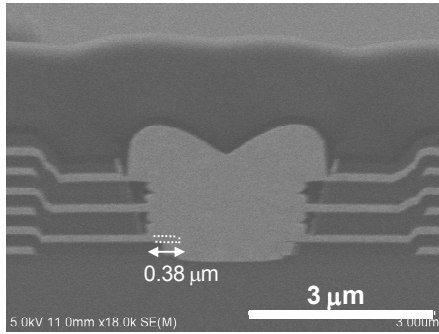
between the through-holes and the small holes in the MIM electrodes. Next, a 100-nm-thick Au seed layer is sputtered, followed by the formation of a photoresist pattern for the through-holes. Then, the through-holes are filled by the electric plating of Au. Finally, the seed layer is removed by $\text{Ar}+\text{O}_2$ inductively coupled plasma (ICP) RIE. This completes the fabrication process for our new stacked MIM capacitor as shown Fig. 1(c). With this process technology, stacked MIM capacitors with higher number of stacks can be made by repeating the structure of the two types of electrodes. Using only two additional masks over the conventional single-layer MIM capacitor, we can fabricate multilayer stacked MIM capacitors because vias with side-contacts are formed in one step, which results in lower cost.

3. Results and Discussion

Figure 2 shows a cross-sectional scanning electron microscope (SEM) image of vias with side-contacts. All MIM electrodes are connected to vias sufficiently. Figure 3 shows the dependence of the side-etching of the



(a) Two through-holes



(b) Enlarged view of a through-hole

Fig. 2. Cross-sectional SEM images of through-hole.

through-hole on the number of layers of MIM electrodes. Precise control of side-etching was achieved with the developed process.

We fabricated three-, four-, and five-layer stacked MIM capacitors with 175-nm-thick SiN. Figure 4 shows the layer-number dependence of capacitance density (C_d). C_d increases in proportion to the number of layers. C_d of the five-layer MIM capacitor is $1.47 \text{ fF}/\mu\text{m}^2$ since the capacitance of each layer is $0.30 \text{ fF}/\mu\text{m}^2$. The leakage currents of the stacked MIM capacitors are lower than the limit of the current-voltage (IV) measurement equipment, indicating that the leakage current is not increased by the vias with side-contacts in the electrodes. Therefore, the stacked MIM capacitors are at a practical level in terms of application to IC chips.

We also fabricated three-layer stacked MIM capacitors with a 130- and 100-nm-thick dielectric layers using same fabrication process. Their capacitance density data are plotted in Fig. 4. The C_d of the 100-nm-thick three-layer MIM capacitor is $1.51 \text{ fF}/\mu\text{m}^2$. The leakage current of three-layer stacked MIM capacitor is 10^{-2} A/F , which is still lower than the limit of the IV measurement equipment. This shows stacked MIM capacitors with a thin dielectric-layer can be fabricated by the proposed process.

4. Conclusion

We fabricated stacked MIM capacitors with side-contact formation technology as a way to increase capacitance density. We demonstrated that the density of MIM capacitors can be increased from $0.30 \text{ fF}/\mu\text{m}^2$ to $1.51 \text{ fF}/\mu\text{m}^2$ (a factor of 5) using our technology. Using these technologies, we are ready to meet the challenge of fabricating extremely compact analog-frontend IC chips.

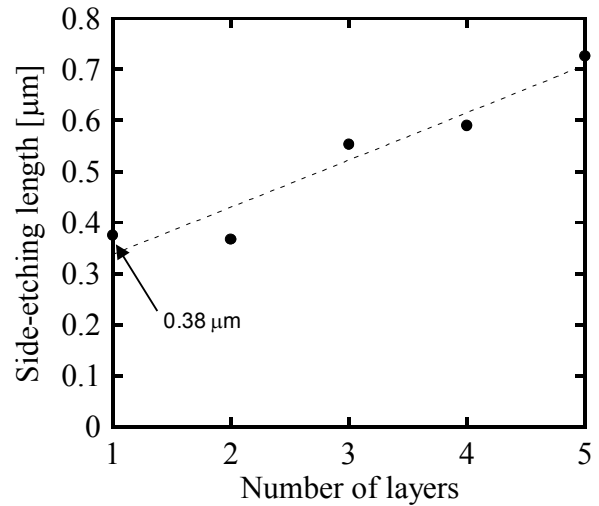


Fig. 3. Layer-number dependence of side-etching of through-hole.

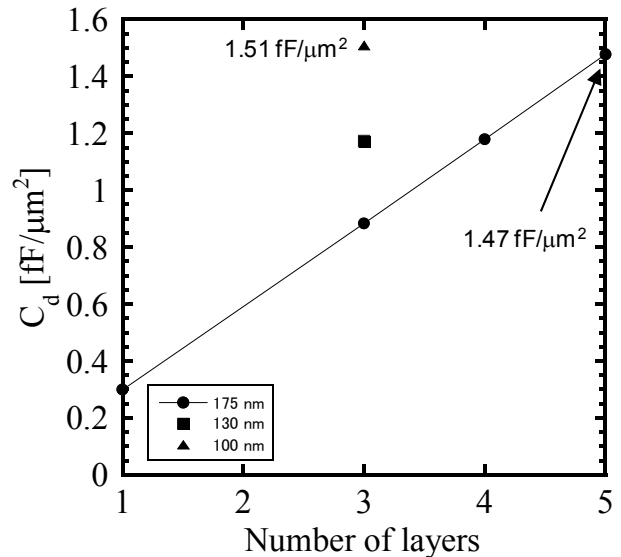


Fig. 4. Layer-number dependence of capacitance.

Acknowledgements

The author thanks S. Yamahata and T. Enoki for their encouragement throughout this work.

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