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Crystalline Silicon Solar Cells, Thinner the Better

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1. Introduction

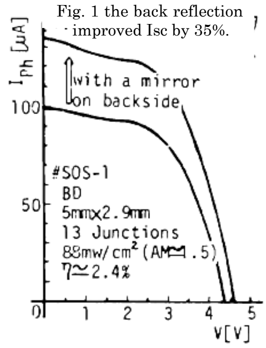
It had long been doubted since 1970's that thin crystalline silicon solar cells with the thickness less than few hundreds of micro-meters can realize a conversion efficiency competitive with "usual" thick counterparts and a potentially lower cost. The doubt came from many professors and researchers who have judged only by "material science". However, to realize high efficiency solar cells, "device physics and technology" play important roles. For instance, the optical path and the electrical path for the carrier transport can be separately designed. Recent (with reference to 1970's) European papers[1] on the "paper thin solar cells" have broken their doubt.

In this paper, the history of the research and development of very and ultra-thin crystalline silicon solar cells and their guiding principle will be presented.

2. Early day proposal

In 1973, a first trial was started to estimate a possibility of the ultra-thin crystalline silicon (cSi) solar cell and the importance of use of the back reflection was demonstrated with a 3 μ m thick small sized solar cell as shown fig. 1[2].

Fig. 1 the back reflection improved Isc by 35%.



By using a model with a constant mobility and constant life time across the cell thickness, ultra-thin solar cells with the back reflection and built-in drift fields were analyzed for low grade silicon and 12.5% peak efficiency was predicted at the thickness of 6 μ m with a diffusion length of 3 μ m[3].

Then, using KOH etching of thick (100) p-type 0.1~0.3 Ωcm CZ cSi wafers (the diffusion length was estimated as 36 μ m), very thin solar cells with the thickness ranging from 12 to 100 μ m was fabricated in 1985 and the results were reported as shown by plot C in fig. 2. .The each cell has boron BSF diffusion, front and back surface passivation by SiO_2, an Al film as a back reflector on the SiO_2 and partial back side contacts through the SiO_2. These features were different from usual cells at that time. Even without anti-reflection coating except for SiO_2 for passivation, 17 % of conversion efficiency with very thin cell thickness i.e. 30 μ m was first verified[4,5].

These results suggested that increase in the cell thickness 2～3 times larger than the minority carrier diffusion length results loss of the conversion efficiency. The thinner cell with the careful optical path design is inevitable for high efficiency with lower grade (low cost) cSi.

3. Thin film challenge

CSG (crystalline silicon on glass) technology[6] was extended to the volume production at Pacific Solar in 1995. A silicon thin film was deposited (1.4~2.4 μ m thick) on a textured glass substrate, dehydrogenated at 500 ℃, solid-phase crystallized at 600℃, followed by 910~930℃ RTA and hydrogen-passivated at 610 ℃. The best mini-module efficiency[7] was 10.4% with Jsc=29.5 mA/cm^2.

The thin film poly-cSi solar cell grown by high temperature (400℃) plasma CVD on a glass substrate was reported[8,9] by Kaneka in 1994~1996. The cell structure is ITO (800nm) /p μ c-Si:H (20nm) /poly-Si (1~10 μ m) /n+ poly-Si (300nm) (/p+ poly-Si (300nm))/glass substrate. For a 6 μ m poly-Si cell, the conversion efficiency of 6.8% with Jsc=24.1 mA/cm was reported[8]. Following the above trial, with a textured back reflector and top textured ITO (named as STAR structure[9]), 10.7 % intrinsic efficiency with Jsc=25.8 mA/cm^2 was realized with the thickness of 2 μ m. In these poly-Si films, poly-Si grains are passivated by a-Si:H and large effective minority carrier diffusion lengths larger than the film thickness is realized.

The conversion efficiency of the thin film poly-Si module will be required to be more than 15 % with low cost for the competitiveness with other thin film modules such as CIS or the alternatives.

3. Very thin wafer challenge

In 2004, Fraunhofer ISE reported very thin wafer (down to 34 μ m) laser fired solar cells[1] (so-called "paper thin" solar cell). They showed that the conversion efficiency of cells fabricated with degraded CZ wafers tends up to 19.5% which is almost same value 20.5% for the cells with a high quality FZ wafer as shown by plot D and F in Fig.2, when the cell thickness approached to the tried minimum value, 34 μ m. Thus, this recent results also verified that with lower grade wafer, high efficiency is obtained by thinning the cell thickness. They tested cracking of the thin wafer during cell process and reported no formidable nor essential issue. IMEC also presented an aggressive roadmap toward further-thin cSi solar cell[10,11].

The etched wafers in the historical experiment[4,5] and the grinded wafers in the above paper[1] were used. However, to make the historical and the above results meaningful, we need a new slicing technology for slicing a Si ingot into low tens of micro-meter thick wafers. Technologies for this very thin slice, free of kerf-loss, are emerging. IMEC reported the stress-induced lift-off method (SLIM cut)[12] and Silicon Genesis Corp announced supply of the very thin cSi wafers (20~150 μm thick) by SiGen cleave process[13,14]. A preliminary cost evaluation by an independent expert on ion implantation physics and equipment on the cleave technology using hydrogen implantation for very thin wafers suggested that the cleave technology is not far from cost ineffective if the wafer thickness is 10 micro-meter or less.

For processing the very thin wafers, transport mechanisms must be improved e.g. use of a thick wafer carrier, a transport sheet, etc and no use of pins to fix nor of tweezers to handle them. We can learn many from preceding wafer handling technology such as for the stacked memory packaging and thin power devices.

Printing or ink-jetting of conductive paste might be used for a module technology, or a low temperature cell process may be applied to array of the very thin wafers on a module substrate.

Fig. 2 shows plots of reported Jsc and efficiency of some of very thin wafer cells and thin film cSi cells with theoretically calculated value[15]. The experimental values are the results from the excellent effort but still have gap to the calculated ones. Voc can be increased with well passivated front and buck surfaces when the cell thickness is reduced. We can set future target of as follows:

cell conversion efficiency: more than 20%

wafer thickness: about 10 micro-meter

BOS cost in the recent high efficiency PV systems occupies about 50 % of total system cost. Then keeping the cell/module efficiency equal to or more than that of conventional thick one is important to keep total cost low. The cost of the poly-Si material and ingot process will be negligibly small, less than 1/20 of the conventional value (10 % + 6 % of the system cost[16]). However, we must prevent the increase in the wafering cost and cell process cost to exceed this earning.

3. Conclusions

Historical trajectory of research and development of the very and ultra thin cSi solar cell/module was reviewed. According to theoretical and experimental reports, more than 20% efficiency with about 10 micro-meter thick cell is one of future targets.

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fig. 2 cell efficiency η and short circuit current, Jsc vs cell thickness