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Study on Device Parameters of Carbon Nanotube FETs to Realize Steep Subthreshold Slope of less than 60 mV/decade

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Abstract

In carbon nanotube FETs (CNFETs) device parameters to observe subthreshold slope (SS) of less than 60 mV/dec have been studied. It is demonstrated, for the first time, that band-to-band tunneling (BTBT) current can be greatly enhanced by reducing the thickness of inter-layer oxide (t_{int}) between substrate and CNT. With a thin t_{int} of 10 nm (SiO_2) and optimized S/D doping, a steep SS of less than 60 mV/dec can be achieved. The physical mechanisms are also discussed.

1. Introduction

In recent years, carbon nanotube FETs (CNFETs) have attracted great attention because of their promising properties and small sizes [1-3]. In fact, thanks to the excellent electrostatics of CNTs, the ideal subthreshold slope (SS) of 60 mV/dec can be expected [2]. Moreover, the IBM group has recently demonstrated SS of 40 mV/dec by utilizing the band-to-band tunneling (BTBT) phenomena [4]. On the other hand, a number of reported CNFETs show SS of greater than 60 mV/dec even in BTBT regime [5,6]. In order to utilize CNFETs as low-power devices, the conditions to realize SS of less than 60 mV/dec need to be clarified.

In this work, characteristics of CNFETs (**Fig. 1**) are investigated for various S/D doping and inter-layer oxide (insulator between the substrate and CNTs) thicknesses (t_{int}). As a result, device parameters to realize SS of less than 60 mV/dec have been obtained. Physical mechanisms for the BTBT optimizations are also discussed.

2. Device Structure & Simulation Method

Device structure used in our simulation is shown in **Fig. 1** [7]. We assume that CNFETs are fabricated on an inter-layer oxide having a conductive substrate underneath. The gate oxide and inter-layer oxide thicknesses are t_{ox} and t_{int}. The portion of CNT uncovered with the electrodes is chemically doped. The diameter of CNT is d_{CNT}.

Full band structures of CNTs are firstly calculated. Utilizing the obtained band parameters, several equations are solved self-consistently [7]. For BTBT, the transmission coefficient through the bandgap is calculated with WKB approximation. The drain current is finally obtained using Landauer's formalism. **Fig. 2** shows the experimental and calculated I_d-V_g characteristics. The excellent agreement including the BTBT region (V_g of less than -0.5 V) demonstrates the validity of our calculation method (BTBT calculation method).

The point of the present simulation is that we included the effect of electrical coupling between the substrate and CNTs. This seems to be a simple effect. However, the effect has not been explicitly taken into account in previous reports.

3. Results and Discussion

The dependence of current-voltage characteristics on t_{int} of devices is firstly examined. **Fig. 3** displays I_d-V_g characteristics of doped-CNFETs with a gate oxide of 1 nm and t_{int} of 10, 50 and 500 nm. For all characteristic shown in this work the source and substrate are grounded. The leakage current, I_{off} of CNFETs is notably enhanced for thinner t_{int}.

In order to investigate the mechanisms for I_{off} enhancement in thinner t_{int}, energy band profiles in CNFETs are drawn as shown in **Fig. 4**. A much steeper band bending is introduced in thinner t_{int} device (Fig. 4(b)), resulting in a shorter BTBT distance and hence a larger BTBT current (I_{off}) in thinner t_{int}. The strong band profile modification by enhanced electrical coupling is due to small density-of-state (DOS) of CNT. Because of small DOS, doped carriers easily repelled from S/D edges in thicker t_{int}. Whereas, the potential in S/D region is pinned by substrate bias in thinner t_{int}. Thus, thinner t_{int} is not good in terms of off-state leakage.

However, it should be noted that CNFETs showing steep SS of 40 mV/dec have thin t_{int} of 10 nm [4]. Therefore, in order to find the device parameter window to observe SS of less than 60 mV/dec, we have modified doping concentration (N_d), since BTBT is a strong function of N_d as well. **Fig. 5** shows I_d-V_g characteristics of CNFETs with t_{int} of 10 nm for various N_d. As N_d decreases, I_{off} is greatly reduced and SS of 50 mV/dec is observed. Again, owing to the small DOS of CNT, channel potential is quite effectively modified by the gate voltage, resulting in steep SS. However, potential profile engineering at S/D edges is critical to have steeper SS. It is found that by combining thin t_{int} and low N_d steep SS is attainable (**Fig. 6**). Bandgap is another parameter to control BTBT. Therefore, careful selection of d_{CNT}, which determines the bandgap of CNTs, is important.

Fig. 7 represents the linear I_d-V_g characteristics of the device having the lowest SS value relatively to the others. **Fig. 8** depicts I_d-V_d curves of the same device. Both figures show that the BTBT CNFET device shows normal transistor characteristics.

4. Conclusions

In summary, we performed detailed simulations for BTBT operation and investigated various parameters of CNFETs. As a method to decrease I_{off} and enhance BTBT current, we propose controlling thickness of inter-layer and doping profile of S/D area. Correspondingly we showed that SS value of less than 60 mV/dec could be obtained in line with our method. However device operation is strongly related with combination of many parameters such as diameter and bandgap of CNTs, potential profile around S/D edge regions, t_{int}, and N_d. Consideration of proper parameters makes CNFETs a good candidate for high performance and low power applications.

References

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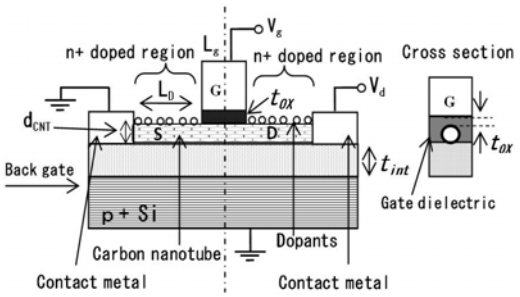

Fig. 1:. Schematic of CNFET structure simulated in this work and cross-sectional view of the structure across the channel direction. CNFET with a doped source-drain is fabricated on inter-layer oxide having conductive substrate underneath. Gate insulator thickness is denoted by t_{ox} and inter-layer thickness by t_{int}.

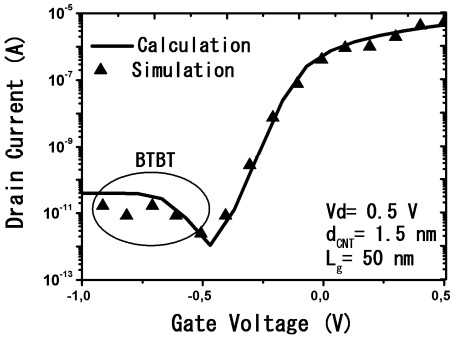

Fig. 2: I_d-V_g characteristics of CNFET with a diameter, d_{CNT}, of 1.5 nm for drain voltage V_d of 0.5 V. Good agreement between calculations and experiments demonstrates the validity of our calculation method. Experimental data are from [2]. The area where BTBT is occurred is depicted.

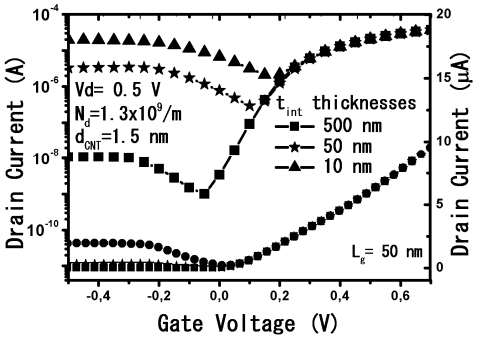

Fig.3: Calculated I_d-V_g characteristics of CNFET with d_{CNT} of 1.5 nm, a gate oxide thickness, t_{ox} of 1 nm and drain voltage of V_d of 0.5 V. The electrical characteristics are simulated for three different inter-layer oxide thicknesses; namely t_{int} of 10, 50 and 500 nm steps.

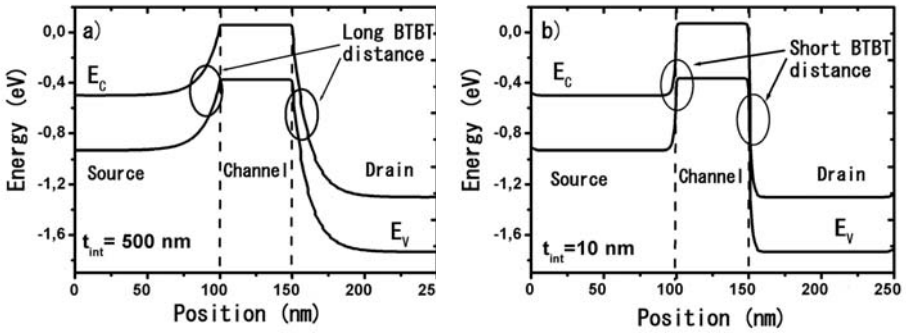

Fig. 4: Energy band profile of (19,0) CNFETs with (a) thicker t_{int} of 500 nm and (b) thinner tint of 10 nm. BTBT distance is decreased in thinner t_{int}, because of the stronger electrical coupling between conductive substrate and CNT in the thinner t_{int} CNFET.

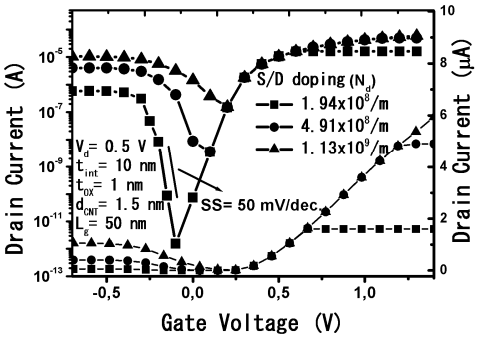

Fig. 5: Calculated I_d-V_g characteristics of CNFETs with t_{int} of 10 nm for three different doping levels from $1.94x10^8$ m^{-1} to $1.13x10^9$ m^{-1}. The sharpest SS value of 50 mV/dec for t_{int} of 10 nm is obtained with the lowest S/D doping profile of $1.94x10^8$ m^{-1}.

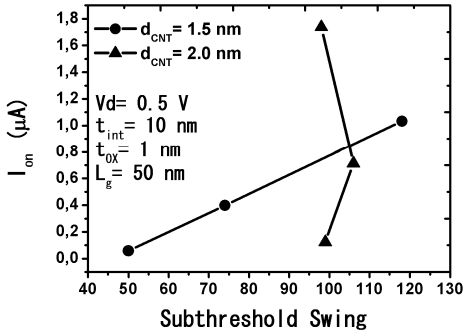

Fig. 6: Subthreshold slope versus ON current, I_{on}, for various CNT diameter, $d_{CNT,}$ of 1,5 nm and 2 nm.

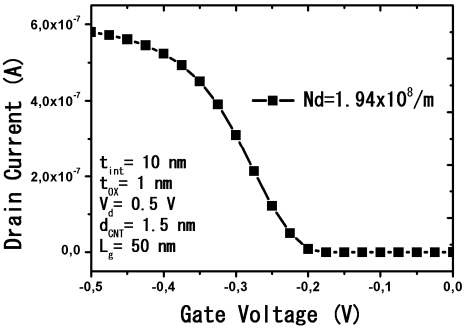

Fig. 7: Linear I_d-V_g characteristics of the CNFET showing the sharpest SS value of 50 mV/dec among the calculated device characteristics.

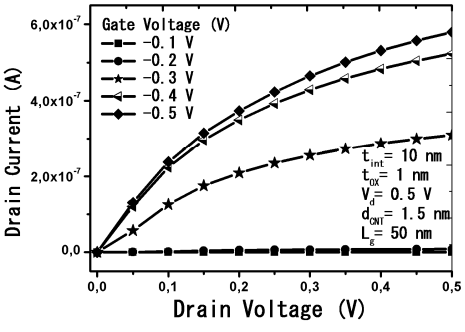

Fig. 8: I_d-V_d characteristics of the same CNFET shown in **Fig. 5** for the case of t_{int} is 10 nm. The gate voltages varies from -0.1 V to -0.5 V with steps of -0.1 V.