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Metal-Catalyst-Free Growth of Carbon Nanotubes for CMOS Integration

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1. Introduction

The excellent electrical, optical, thermal, and mechanical properties of carbon nanotubes (CNTs) have spurred the development of many practical applications including nano-electronic devices [1], biosensors [2], and via interconnects [3]. For applications such as sensors, compatibility of the growth method with Si front-end processing is highly desirable [4] because it provides additional flexibility of a manufacturing process for CNT smart sensors fully integrated with CMOS circuits. CNT growth traditionally involves the use of metal nanoparticles as a catalyst. However, the integration of metal catalyzed CNT growth with CMOS manufacturing process is problematic due to the metal contamination.

Several different metal-catalyst-free growth methods of CNTs have been reported [5-9]. However none of the growth methods can grow single walled CNTs (SWNTs) on SiO_2 for device applications. More recently, Liu et al. [10] and Huang et al. [11] separately reported the growth of SWNTs from SiO_2 nanoparticles formed by scratching the surface of a SiO_2 layer. Whilst the growth of SWNTs on SiO_2 is possible via this method, "scratching growth" is unlikely to be used in Si processing due to the degradation of reliability.

In this paper, metal-catalyst-free growth of CNT using a thin Ge film is reported and this growth process is used to produce back gate CNTFETs with Pd source/drain (S/D) contacts. The novel growth process uses nanoparticles produced by Ar annealing of the Ge film on a SiO_2 layer. Raman measurements show that radial breathing mode (RBM) peaks are present and the disorder induced D-band is absent in our samples, indicating defect-free SWNTs. Electrical measurements on completed CNTFETs show p-FET behavior, an excellent I_{on}/I_{off} ratio of 10^7, and a steep sub-threshold slope of 140 mV/dec.

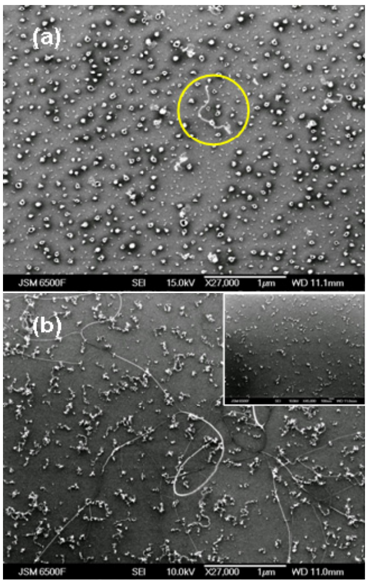

Fig. 1 FE-SEM images after CNT growth from a Ge film on SiO_2 substrate without (a) and with Ar annealing (b).

2. Experimental

A p^+ Si substrate (0.005 Ω·cm) was employed as a back gate and a 45 nm-thick thermally grown SiO_2 layer was employed as a gate dielectric. A 3 nm-thick Ge layer was deposited by either sputtering or evaporation on the SiO_2 layer. The nanoparticles were formed at 850°C for 20 min in a mixture of Ar (1000 sccm) and H_2 (300 sccm) after a pre-annealing in H_2 (1000 sccm) at 950°C. The samples were taken out from a furnace and then growth of CNTs was performed using CVD in a hot-wall reactor at atmospheric pressure. CNTs were grown at 850°C for 20 min using a mixture of methane (1000 sccm) and H_2 (300 sccm) immediately after a pre-annealing in H_2 (1000 sccm) at 900°C. For comparison, CNT growth without the Ar annealing process was also carried out. Back gate CNTFETs were fabricated with Pd S/D contacts. Pd was deposited by sputtering and the S/D electrodes were formed using direct write laser lithography and lift-off. The gap between the S/D electrodes was 2.0 μm and the width was 5.0 μm. Electrical characteristics of CNTFETs were measured in ambient air. Raman spectra were obtained using He-Ne (632.8 nm) laser excitation.

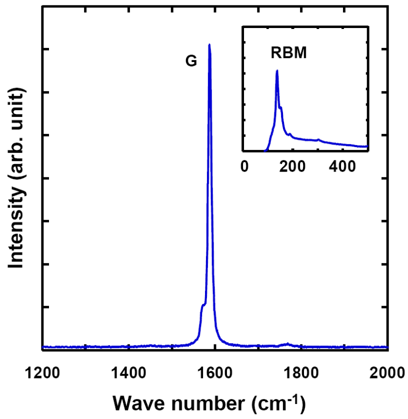

Fig. 2 Raman spectra of CNTs grown from a Ge film on SiO_2 substrate. The inset shows radial breathing mode, indicating that SWNTs are present.

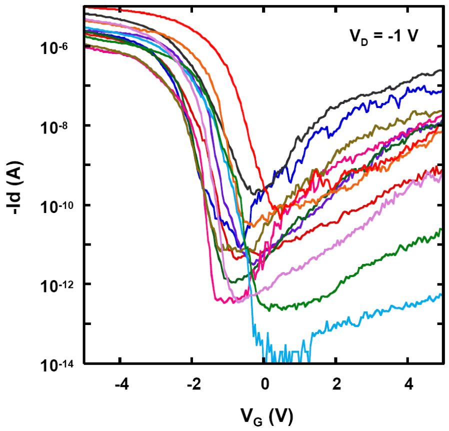

Fig. 3 The sub-threshold characteristics of Pd contacted back gate CNTFETs (L_G = 2.0 μm) with SiO_2 gate insulators.

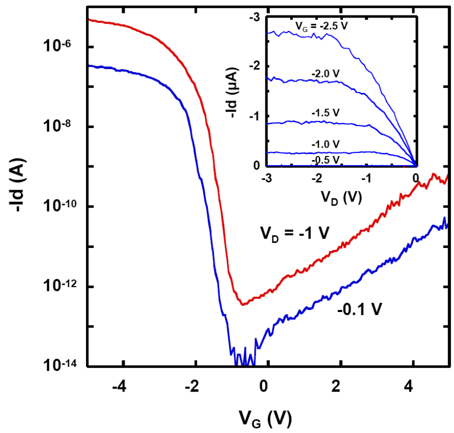

Fig. 4 I-V characteristics of a Pd contacted CNTFET (L_G = 2.0 μm). Sub-threshold characteristics for V_D = -0.1 and -1.0 V and output characteristics for V_G = -0.5, -1.0, -1.5, -2.0, -2.5 V.

3. Results and Discussion

Fig. 1 shows FE-SEM images after CNT growth without (a) and with Ar annealing (b). For samples without Ar annealing, many nanoparticles with diameters around 10 and 50 nm are scattered and EDX analyses indicate that they contain Ge, Si, and O. No CNTs are presented and only isolated nanowires are occasionally seen as shown in Fig. 1(a). Similar nanowires were seen in our earlier work and were composed mainly of silica [7], [9]. In contrast, an additional Ar annealing process dramatically aids CNT growth, giving an area density of 3.0 CNTs/μm^2. Many silica nanowires are also seen. The inset of Fig. 1(b) shows an FE-SEM image just after Ar annealing. Nanoparticles and short nanowires are seen. The nanoparticles were evaluated by means of AFM. Line analyses showed a mean particle density of 450 particles/μm^2 and a particle height of 1.4±0.8 nm. These particles are considered to be GeO_2 or SiO_2 as we have previously reported that silica nanostructure was formed from Ge dots by Ar annealing [12]. The source of oxygen comes from the substrate in this case. The growth of CNTs from the oxide nanoparticles is achieved in the same way as [10], [11].

Fig. 2 shows Raman spectra and the insets clearly show the RBM peaks, indicating that SWNTs are present. All samples show no D-band peak, indicating a low defect density and are thus of high quality. RBM peaks with different Raman shifts within the range from 190 cm^{-1} to the lower limit of 120 cm^{-1} which imposed by our Raman notch filter have been seen. SWNTs observed by Raman scattering have diameters in the range of 1.3-2.0 nm.

Electrical measurements of the Pd contacted back gate CNTFETs have been made on more than 80 functional devices. Fig. 3 shows sub-threshold characteristics for twelve typical CNTFETs. The drain current at V_G=-5 V and V_D=-1 V ranges from 1 to 10 μA and I_{on}/I_{off} ranges from 10^4 to 10^8. Fig. 4 shows one of the best electrical characteristics of CNTFETs exhibiting an excellent I_{on}/I_{off} ratio of 10^7 and a reasonably steep sub-threshold slope of 140 mV/dec. The output characteristics show linear characteristics below saturation (V_D>-1 V) and good saturation (V_D<-1 V).

4. Conclusions

We have developed a CMOS compatible CNT growth method on a SiO_2 substrate using a Ge thin film. The synthesized CNTs were successfully applied to fabricate back gate CNTFETs with Pd S/D contacts. The CNTFETs have an excellent on/off current ratio of 10^7 and a steep sub-threshold slope of 140 mV/dec.

Acknowledgements

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