

Performance Potentials of Bilayer Graphene and Graphene Nanoribbon FETs

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1. Introduction

Graphene, a one-atom-thick carbon sheet arranged in a honeycomb lattice, is expected as a candidate material for use in channels of next-generation FETs, because of the extremely high mobility and the easy control of charge carriers by applying a gate voltage [1]. However, an important drawback of graphene regarding FET application is the lack of bandgap. Therefore, the electrical conduction cannot be fully switched off by tuning the gate voltage, which is necessary for digital applications. As a way to overcome this drawback, several methods of opening a bandgap have been proposed: (I) patterning monolayer graphene into nanoribbon (graphene nanoribbon: GNR) [2,3], and (II) utilizing bilayer graphene (BLG) placed in an electric field perpendicular to BLG [4] or introducing symmetry breaking between the two carbon layers via, such as interaction between graphene layer and substrate [5,6]. In this paper, we project performance potentials of BLG- and GNR-FETs based on a first-principles approach, and perform a comparative study between both FETs.

2. Bandstructures

Fig. 1 shows the atomic models used in the simulation. For the BLG simulation, we introduced breaking of the A and B sublattice symmetry due to an atomic displacement as shown in Fig. 1 (a) and (b), where we examined two kinds of displacements, that is, horizontal displacement in (a) and vertical displacement in (b). The blue arrows denote the actual displacement orientation applied to carbon atoms. As shown later, the vertical displacement opens a bandgap identical to that induced by the electric field [7,8]. For GNR, we focused on armchair-edged GNR shown in Fig. 1 (c), because it has a bandgap when $N=3m$ or $3m+1$, where m is an integer [9,10]. In Fig. 1 (d), the Brillouin zone (BZ) in k-space is depicted, along with the 1D-BZ for GNRs.

Fig. 2 shows the bandstructures computed for (a) graphene, (b) the BLGs and (c) the GNRs. The calculations were performed using the Vienna *ab initio* simulation package (VASP) [11], within the GGA interactions. Zooming in on the Dirac point in Fig. 2 (b) reveals that due to the symmetry breaking caused by vertical displacement (ϵ_z), a bandgap of 0.14 eV is opened and a *Mexican hat* structure with negative effective mass appears in the low-energy spectrum of BLG. The above results are almost-entirely identical to those of the electric field (gate) induced approach [4,7,8]. In addition, we found that the bandgap linearly increases with ϵ_z and takes the maximum value of 0.14 eV at $\epsilon_z = 7\%$, as shown in Fig. 3 (a). Hence, we will use the BLG-channel with $\epsilon_z = 7\%$ hereafter.

The GNRs also have a bandgap as shown in Fig. 2 (c),

which greatly depends on the ribbon width as shown in Fig. 3 (b) [10,12]. Here, it is particularly worth noting that a linear dispersion nature still remains in the wide GNR with $W = 4.3$ nm, regardless of opening a finite bandgap of 0.18 eV [12]. Its linearity can be clearly confirmed in Fig. 4, where normalized dispersion curves near conduction band minimum for BLG and GNRs are compared. Thus, a higher carrier velocity than those of BLGs is expected, especially in wide GNRs as presented in the next section.

3. Electrical Properties

Fig. 5 shows the schematic diagram of the simulated graphene FETs. The source and drain are assumed to be heavily doped BLG/GNR contacts while the channel is intrinsic. Fig. 6 shows (a) $I_D - V_G$ characteristics and (b) intrinsic device delays versus the ON-OFF current ratio, which were computed using the “top-of-the-barrier” ballistic model [12,13]. It is found that the GNR-FETs provide not only the larger drain current, but also the smaller intrinsic delay than the BLG-FET, which are anticipated by the fact that the BLG-channel has the Mexican hat structure in its dispersion relation, leading to a negative effective mass as described above. However, the performance potential of the BLG-channel FET is found to be comparable with that of InP-HEMTs [8] as shown in Fig. 7. Considering its feasibility of practical manufacturing with less variability as compared to GNR, BLG is also promising as a post-Si channel.

4. Conclusions

Based on the first-principles and ballistic approach, we have found that GNR-FETs with ribbon width of about 3 ~ 4 nm exhibit better device performance than n-channel Si-MOSFETs and InP-HEMTs. Although the BLG-FET shows inferior performance potential compared to the GNR-FETs with similar bandgap, it is still comparable with that of InP-HEMTs. Therefore, GNRs and BLGs with a finite bandgap are both expected to be promising channel materials for future high-speed digital switches in VLSIs.

Acknowledgements This work was partially supported by the Semiconductor Technology Academic Research Center (STARC).

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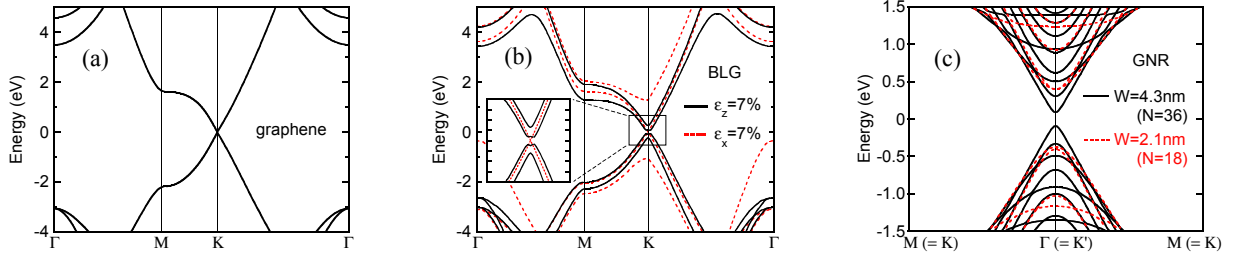
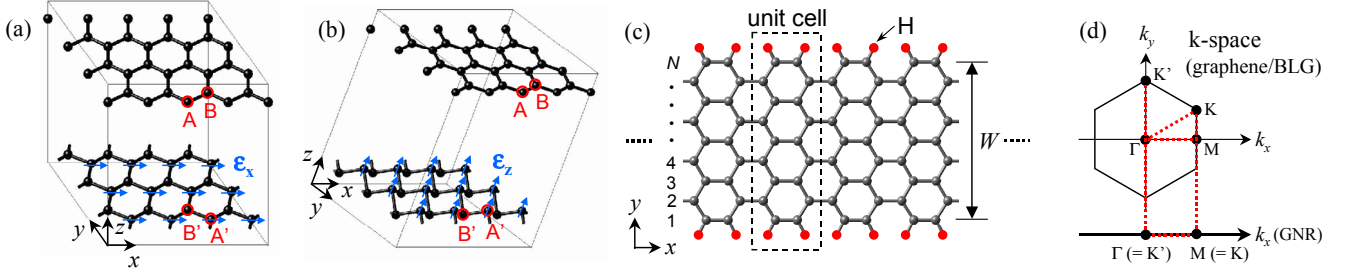


Fig. 2 Bandstructures computed for (a) graphene, (b) BLGs and (c) GNRs. In (b), the results for horizontal and vertical atomic displacements with $\epsilon_x = \epsilon_z = 7\%$, and in (c) the results for two ribbon widths for $W = 4.3\text{nm}$ and 2.1nm are plotted.

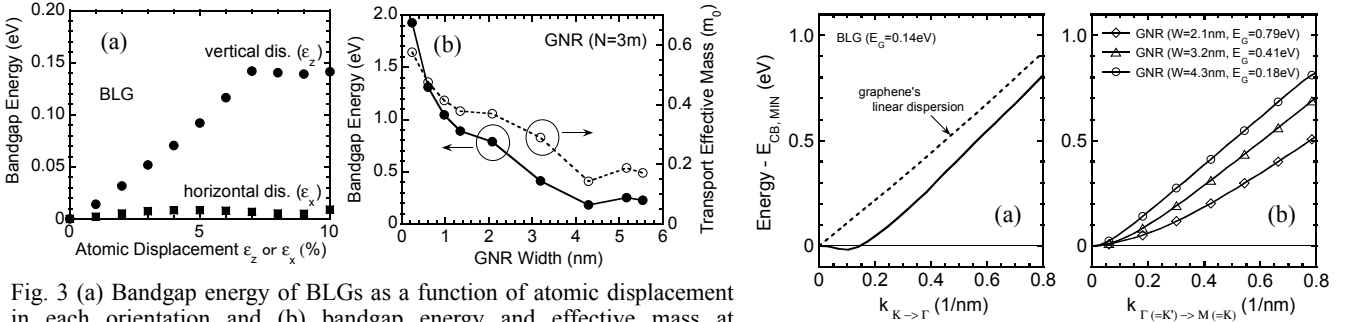


Fig. 3 (a) Bandgap energy of BLGs as a function of atomic displacement in each orientation and (b) bandgap energy and effective mass at conduction band minimum of GNRs as a function of ribbon width.

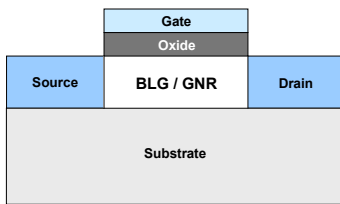


Fig.5 Diagram of the simulated graphene FETs.

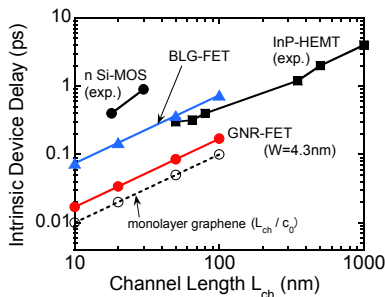


Fig. 7 Simulated intrinsic device delays of GNR- and BLG-FETs with similar bandgap, as a function of channel length. Experimental extrinsic values of n Si-MOSFETs and InP-HEMTs [8] are also plotted. $I_{ON}/I_{OFF} = 10^4$.

Fig. 4 Comparisons of dispersion curves near conduction band minimum for (a) BLG with $E_G = 0.14\text{eV}$ and (b) GNRs with three different ribbon widths. In (a), the graphene's linear dispersion is also plotted for comparison.

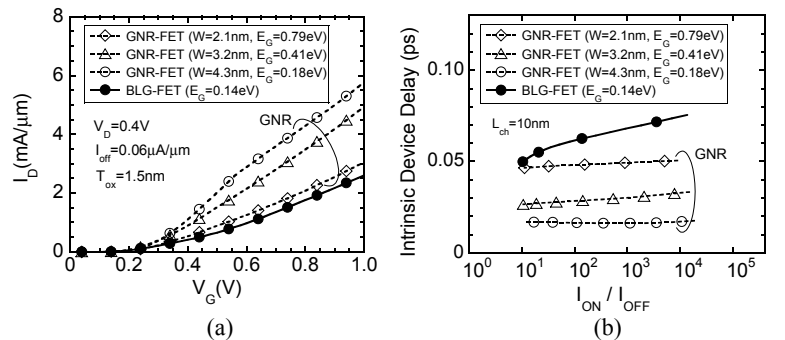


Fig. 6 (a) I_D - V_G characteristics and (b) intrinsic device delays versus I_{ON}/I_{OFF} ratio for GNR-FETs with three ribbon widths and BLG-FET with the maximum bandgap of 0.14eV due to $\epsilon_z = 7\%$. $V_D = 0.4\text{V}$ and $T_{ox} = 1.5\text{nm}$. In (a), the simulations are performed at the same OFF-current density ($I_{off} = 0.06\mu\text{A}/\mu\text{m}$). In (b), the channel length is assumed to be 10nm , and the intrinsic device delay is calculated as $\tau = (Q_{ON} - Q_{OFF}) / I_{ON}$, where Q_{ON} and Q_{OFF} are total charge in the channel at ON- and OFF-states, respectively, and I_{ON} is ON-current.