Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp880-881

Epitaxial Graphene-On-Silicon Logic Inverter

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1. Introduction

Graphene, a single layer of graphite, has recently attracted a huge attention due to its promising properties [1]. Constructing high-performance digital units using graphene has been a real challenge, and several logic graphene inverter devices have been demonstrated [2, 3]. However, their performances are still far away from the practical requirements. Some of the challenges are the unmatched output/input bias and the need of high power supply [2].

In this work, we report on the complimentary logic inverter, using two back-gate epitaxial graphene-on-silicon field-effect transistors (GOSFETs) [4] at room temperature.

2. Experimental setup

The epitaxial graphene is formed on the surface of a 3C-SiC(110) layer grown on a Si(110)-oriented substrate. The starting material is a B-doped, p-type Si wafer, cut to 7 x 40 mm^2 in size [5]. After ex-situ wet cleaning, the sample is loaded into the reactor and flash-annealed in vacuum at 1200 ^oC for several times to obtain a clean surface. After in-situ cleaning, the 3C-SiC is grown by gas-source molecular beam epitaxy (GSMBE) using monomethyl silane (MMS) at a pressure of 3.3 x 10^{-3} [6]. The SiC growth starts with a buffer-layer formation (600 ^oC for 5 min) and a subsequent SiC growth (1000 ^oC for 120 min). For this growth condition, the thickness of the SiC layer is typically 80 nm. After that, MMS is exhausted from the reactor and the sample is annealed in vacuum at 1200 ^oC for 30 min to form graphene on the surface of the SiC layer.

The device fabrication starts with the ohmic contact formation. First, the source/drain electrodes consisting of 30 nm thick Ti and 100 nm thick Au are deposited on the FLG sample and patterned by a liftoff process. The active FLG layer is then defined using standard g-line lithography with a mask aligner and the sample is exposed to low-energy oxygen plasma to remove the FLG layer except the device active area.

Two neighboring GOSFETs have been used to form a single complimentary graphene-on-silicon (CGOS) logic inverter. The input bias (V_{IN}) was applied through the back gate, and the output bias (V_{OUT}) was extracted from the common drain of the two FETs. The source of one GOSFET was grounded and the source of the other was connected to a conventional CMOS supply voltage (V_{DD}). All measurements were done at room temperature.

3. Results and discussion

The obtained GOSFETs exhibited a significant gate leakage current, which indicates that the measured drain current includes also the gate leakage current [7]. A model has been used to extract the drain to source current by de-embedding the gate leakage from the measured drain current [7]. Fig. 1 shows the transfer current of the GOSFET after applying the model.

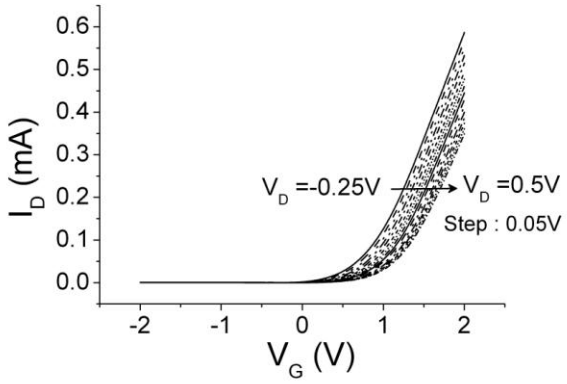

Fig. 1 The transfer current obtained after applying the model.

Fig. 2 shows that when applying a negative drain bias, the Dirac point was shifting on the negative side as well, while it was almost constant for positive drain bias. The ambipolar properties have been observed in our device, even though the drain current in the p-type side looks significantly lower than the n-type side as shown in Fig. 2.

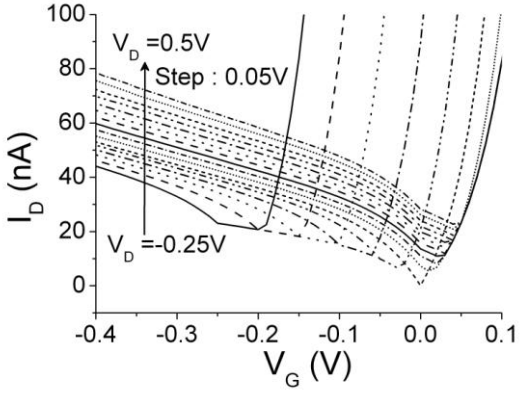

Fig. 2 The positions of the Dirac points depending on the drain bias.

After measuring the transfer characteristics (V_{OUT} vs. V_{IN}) of our CGOS device, we applied the compensation model, by de-embedding the gate leakage from the channel currents of the GOSFETs on both the V_{DD} side and on the source side (Inset Fig. 3), then we recalculated both resistances R_{DD} and R_S. Finally, V_{OUT} was determined using eq. (1):

$$V_{OUT} = \frac{V_{DD}}{1+\frac{R_{DD}}{R_S}} \qquad (1)$$

The obtained transfer characteristics (V_{OUT} vs. V_{IN}) for the CGOS device exhibited good inverting operations with a matched output/input voltage ranging from 0 to 0.1V for V_{DD} = 0.1V, and from 0 to 0.5V for V_{DD} = 0.5V as shown in Fig. 3. Besides, the inverting operations of the CGOS device were obtained at as low V_{DD} bias as 0.1V. The top peak zone of the transfer curve can possibly be used in order to obtain XOR, NAND and OR logic operations [3].

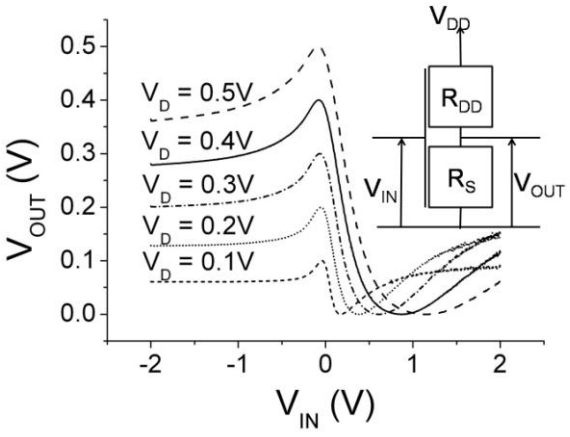

Fig. 3 The obtained transfer characteristics of a CGOS device for different values of V_{DD}. The inset is a schematic of the CGOS device

Moreover, for a similar CGOS structure, based on ambipolar GOSFETs, the results of the theoretical simulation were relatively in good agreement with the experimental results (Fig. 4).

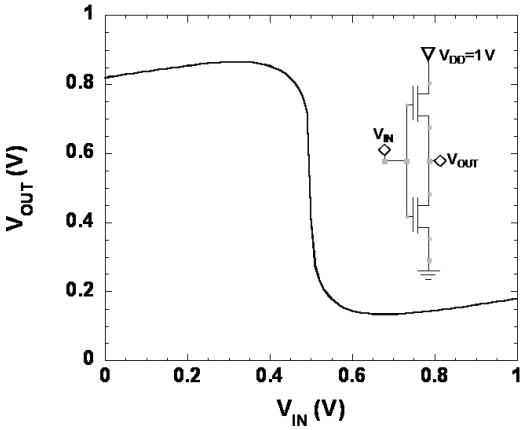

Fig. 4 The calculated transfer characteristics of a typical CGOS for V_{DD} = 1V.

4. Conclusions

Epitaxial CGOS logic inverters have been fabricated and investigated. Although, a large amount of gate leakage current was observed, the inverting operations of the CGOS device at as low V_{DD} bias as 0.1V, with a matched output/input voltage, were obtained by de-embedding the gate leakage from the drain current. The suppression of the gate leakage current and the use of the top gate bias [2] may be the key to high performance CGOS devices.

Acknowledgements

This project is supported by JST-CREST. The device processing in this work was carried out at the Laboratory for Nanoelectronics and Spintronics in the Research Institute of Electrical Communication, Tohoku University.

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