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Observation of bandgap in epitaxial bilayer graphene field effect transistors

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1. Introduction

Graphene, a monolayer of graphite, has gained an enormous amount of attention because of its intriguing physical properties [1]. Its high carrier mobility [2] suggests that it would be useful as a future electronics material. Graphene is obtained by mechanical exfoliation of graphite [3]. However, this technique is only good for making graphene flakes of only a few dozen microns in diameter. A method for producing larger graphene sheets is necessary for its industrial applications. Thermal decomposition of silicon carbide (SiC) [4] is a promising approach to make such sheets.

A number of reports have shown that epitaxial graphene on an SiC substrate can act as channels for field effect transistors (FETs) without the need to transfer it onto insulating substrates. Recently, SiC graphene-based FETs operating at a frequency of up to 100 GHz have been reported [5]. However, regardless of how graphene is fabricated, the on/off ratio of graphene FETs has been too small for realistic usage. The poor on/off ratio is due to the zero-gap characteristic of monolayer graphene. Bilayer graphene, on the other hand, may be able to give a high on/off ratio since a bandgap can be formed with it by breaking the inversion symmetry of the two layers [6]. Indeed, bandgap openings were observed in electron-doped bilayer graphene by angle-resolved photoemission spectroscopy (ARPES) [7] and in dual-gate bilayer graphene FETs by measuring electronic transport properties [8]. Although gap opening was confirmed electronically in mechanically exfoliated bilayer graphene FETs [8], no such report has been made for epitaxial graphene. Here, we report on observation of a bandgap in top-gated graphene FETs, in which epitaxial bilayer graphene was used as channels.

2. Experimental

Bilayer graphene was grown on a commercially available semi-insulating 4H-SiC(0001) substrate in a UHV environment. The substrate was annealed by electron-beam bombardment from the backside of the substrate. The annealing temperature was about 1270℃. The thickness of the graphene layers formed on the substrate was analyzed by low energy electron microscopy (LEEM) [9]. As shown in Fig. 1 (a), bilayer graphene continuously covered most of the region, with islands of one to four layers forming in some areas. Since these islands were localized, the bilayer graphene was the dominant carrier transport layer.

Figure 1(b) is a schematic illustration of a fabricated FET. The device had a top-gate configuration and was fabricated by defining the channels at the beginning of the process. The channels were designed such that the transport characteristics of channels parallel and perpendicular to the steps could be studied (Fig. 1 (c)). The channels were formed by using photolithography to prepare an etching mask on the graphene. Reactive ion etching in a CF_4 and O_2 atmosphere was then performed to etch the unmasked graphene layer and this was followed by removal of the mask in warm acetone. After that, 85 nm of hydrogen silsequioxane (HSQ) and 40 nm of SiO_2 were respectively spin-coated and sputtered onto the whole substrate to form a dielectric layer. To make electrical contacts for the graphene channels, the dielectric layer above the contact pads was removed by HF etching. During the etching, all areas except those above the contact pads were protected by a photoresist layer. Finally, electrodes were patterned by using photolithography, Cr/Au (10/200 nm) evaporation, and a lift-off process. The graphene channels aligned parallel to the substrate steps were used for this study. The channel width and length were 2.5 μm and 7.5 μm, respectively. Four terminal measurements at temperatures between 2 K and 300 K were carried with a constant current of 1 μA.

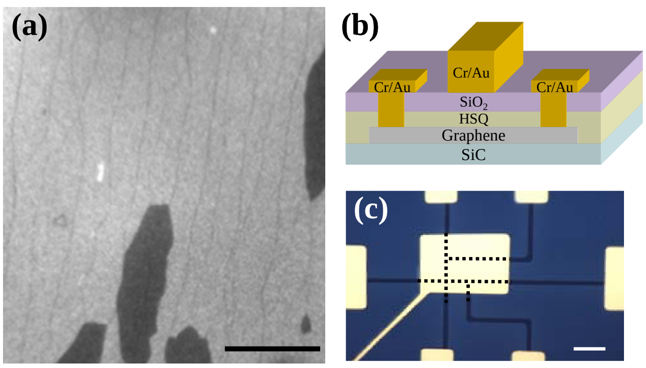

Fig. 1 (a) LEEM image of the bilayer graphene (gray area). White spots and black areas are monolayer and trilayer graphene, respectively. Vertical lines are substrate steps. Scale bar is 1 μm. (b) Schematic cross-sectional view of the fabricated FET (c) Photograph of the fabricated FET. Dotted lines indicate graphene channels under the top-gate electrode. The horizontal channels are parallel to the steps.

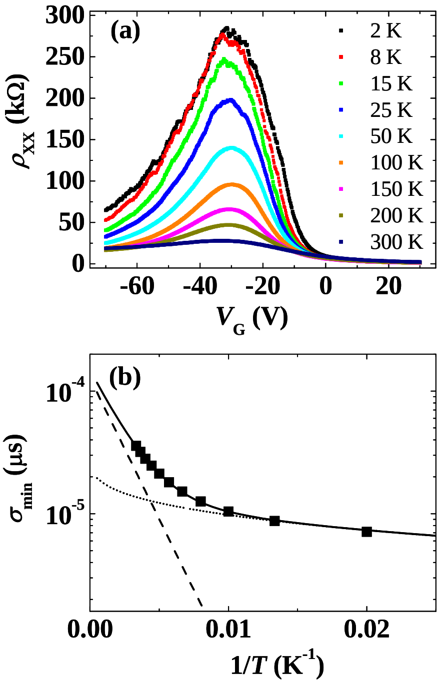

Fig. 2 (a) Temperature dependence of the resistivity (ρ_{XX}) as a function of gate voltage. (b) Temperature dependence of the minimum resistivity σ_{min} (black squares). The dashed and dotted lines are fits reflecting only thermally activated behavior and variable range hopping behavior, respectively. The solid line combines both behaviors.

3. Results and discussion

Figure 2 (a) shows the transfer characteristics of the device. The carrier density in the graphene could be controlled by sweeping the gate voltage (V_G). In principle, the charge neutrality point (Dirac point) should be at $V_G = 0$ if the graphene is undoped. In our case, the Dirac point was at $V_G =$ ～-30 V, judging from the value of the gate voltage at maximum resistivity. This indicates that the graphene was *n*-doped. Intrinsic electron-doping is a characteristic of graphene grown on SiC, and it is due to charge transfer from the substrate [7]. The figure shows a strong temperature dependence of the resistivity at the Dirac point. Here, if we define the on/off ratio as the ratio of resistivity at the Dirac point and resistivity at $V_G = 30$ V, it is 29 and 291 at 300 K and 2 K, respectively. Hall effect measurements were carried out to estimate the carrier mobility and the carrier density. The carrier mobility was weakly dependent on temperature, and it was 800 $cm^2V^{-1}s^{-1}$ at 6×10^{12} cm^{-2} from 2 K to 150 K. Carrier mobility tended to decrease with decreasing carrier density, which is similar to the case of exfoliated bilayer graphene [10]. From the results of the LEEM measurement and the Hall effect measurement, we concluded that the bilayer is the dominant channel for carrier transport. Accordingly, the large on/off ratios and strong temperature dependence of the maximum resistivity indicated bandgap opening in the graphene.

We quantitatively evaluated the size of the bandgap from the temperature dependence of the maximum resistivity. First we tried to apply a thermally activated transport model in which the minimum conductivity σ_{min} is proportional to $\exp(-E_a/k_BT)$, where E_a is the activation energy and k_B is the Boltzmann's constant. However, the model failed to fit the data in the entire temperature regime. It has been reported that the presence of localized states between the conduction band and the valence band will cause variable range hopping in the low temperature region such that σ_{min} is proportional to $\exp(T_0/T)^{-1/3}$, where T_0 is a characteristic temperature [8]. Figure 2 (b) shows the results of a fitting taking account of both thermally activated transport and variable range hopping. A bandgap of 90±4 meV was obtained under the assumption that the bilayer graphene is an intrinsic semiconductor, where E_a is half the bandgap. This value needs further verification because the dielectric layer on the graphene surface and (or) presence of charged impurities in the dielectric layer, for example, may have masked the true bandgap of the graphene. Therefore, we cannot directly compare our result with the ARPES result [7] at this moment. However, our results indicate that we can use electronic transport measurements to analyze the bandgap in epitaxial bilayer graphene.

4. Conclusions

We fabricated top-gate FETs, in which the channels were bilayer graphene grown on a SiC substrate. By applying a top-gate bias, we could control the carrier density and shift the Fermi level of the graphene. The experimental large on/off ratios and strong temperature dependence of the maximum resistivity suggest bandgap opening in these SiC graphene FETs. Although a more detailed analysis is needed to confirm the exact magnitude of the bandgap, we obtained a preliminary value of 90 meV by considering thermally activated transport and variable range hopping.

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