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# Effect of oxidation-induced tensile strain on Gate-all-Around silicon nanowire based single-electron transistor fabricated using optical lithography

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## 1. Introduction

Silicon single-electron transistors (SETs) are promising building blocks for future high-density and low-power integrated circuits [1-2]. Electron beam lithography (EBL) is commonly used for the fabrication of SETs to achieve device dimension of less than 10 nm needed for room temperature operation [3-6]. This imposes a challenge for mass production. In this paper, Silicon nanowire (SiNW) based SETs operating at room temperature are realized through thermal oxidation of Si fins fabricated with conventional optical lithography. This is advantageous since it bypasses the inefficient electron beam lithography and has better compatibility with existing well-developed Si process, which allows integration with CMOS devices.

The mechanism of formation of tunneling barriers in SiNWs based SETs is still under discussion [1, 7]. The most likely mechanism involves a combination of expansion of bandgap due to the quantum confinement, and shrinkage of bandgap due to the oxide-induced strain [7, 8]. To realize SET devices for room temperature operation, it is important to develop a good understanding of the tunneling barrier formed. In this work, the effects of different oxidation-induced tensile strain on the formation of tunneling barriers in SiNW based SET are investigated. It is verified that the mechanism in forming SET in SiNW is the combination of barrier lowing due to the strain, and the barrier increase due to quantum confinement in extremely small nanowire. The fabricated devices are N-type gate-all around (GAA) SiNW MOSFET with 3 to 4 nm channel. Different tensile strain induced on the SiNW was achieved by designing nanowires with different lengths. Investigation on oxidation-induced strain on gate-all-around nanowires based on Micro-Raman spectroscopy has shown that the induced strain increases for longer SiNWs [9].

## 2. Device fabrication

Alternating phase shift mask lithography with KrF scanner, plasma resist trimming and dry etching were used to define the Si-fins with 40 nm to 43 nm width and 200 nm to 500 nm lengths on 8 inch SOI wafer (100) [10]. The top Si layer is p-type with a thickness of 200 nm and doping of $10^{15}$ $cm^{-3}$. The patterned Si was then oxidized in dry oxygen at 875 ºC for 4 hours, results in two Si nanowires [10]. The top SiNW was etched away by dry etching and bottom one was released from oxide by DHF solution. 4 nm $SiO_2$ was then grown and 130 nm LPCVD amorphous Si (α-Si) was deposited as gate [10]. The gate was defined longer than the wire length, 70 nm oversize on each edge to avoid misalignment during lithography. It was followed by gate pattern transfer and Source/Drain implantation, activation annealing at 950 °C and standard metal contact formation. The final SiNW channel has a width of 3 nm to 4nm for different starting fin widths. Overview of a device with Si-fin of 43 nm before oxidation is shown in Fig. 1 and inset shows the device has a SiNW cross section of 4 nm.

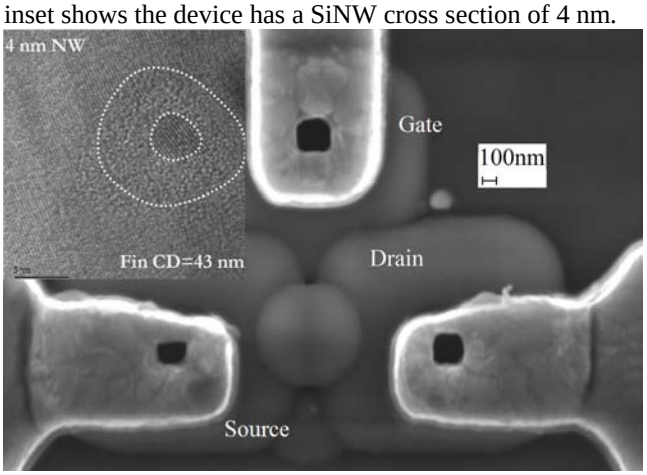


Fig. 1 SEM micro view of the entire device. SiNW between S/D pad with 400 nm length was encapsulated by 130 nm thick LPCVD α-Si gate. Inset: TEM view of SiNW cross section with 4nm diameter after oxidation and α-Si gate deposition. The inner and outer circles indicate the contours of the SiNW and the encapsulating gate oxide.

## 3. Device characterization and discussion

Fig. 2 shows the drain current versus gate voltage ($I_D$-$V_G$) of the fabricated device with a SiNW width 4 nm at different temperatures. Drain voltage was fixed at 1 mV. The length of the SiNW is 400 nm. Clear oscillation peaks are observed under room temperature which indicates the device is operating in the Coulomb blockade regime and SETs are successfully fabricated using optical lithography without EBL [11]. To observe Coulomb blockade, the charging energy of a SET device must be much larger than the thermal energy *kT*. For our devices, we attribute the high charging energy to their extremely small dimension.

The devices were also characterized at 77 K and 150 K. Clear Coulomb oscillations are observed at low temperatures, and an increase in the peak-to-valley ratio is noted with decreasing temperature. This further confirms single electron transport in the devices because lower temperature

will lead to a lower thermal energy $kT$ and hence accentuated Coulomb blockade effect [12].

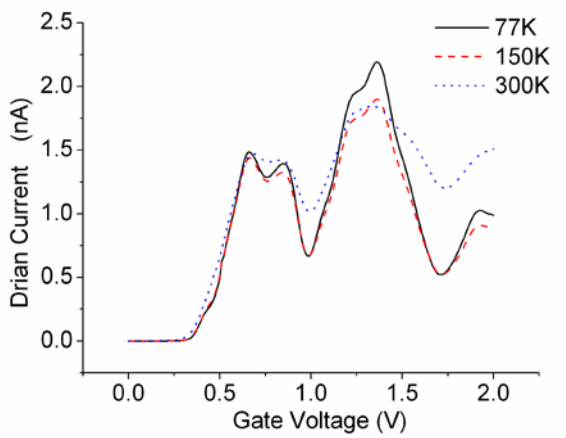


Fig. 2 $I_D$ - $V_G$ of the fabricated device with a SiNW width of 4 nm at various temperatures. Clear Coulomb blockade oscillation is observed under room temperature. It is also noted that and Peak-to-Valley ratio increases as temperature lower down.

Fig. 3 shows the room temperature $I_D$-$V_G$ characteristics of several devices with different SiNW lengths. The width of SiNWs is 3 nm. It is interesting to observe that Coulomb blockade oscillations are dependent on the length of the SiNWs. The amplitudes of the oscillations are reduced with decreasing length from 500 nm to 250 nm. When the length is further reduced to 200 nm, no oscillation is seen and the $I_D$-$V_G$ curve reverts to that of a typical MOSFET.

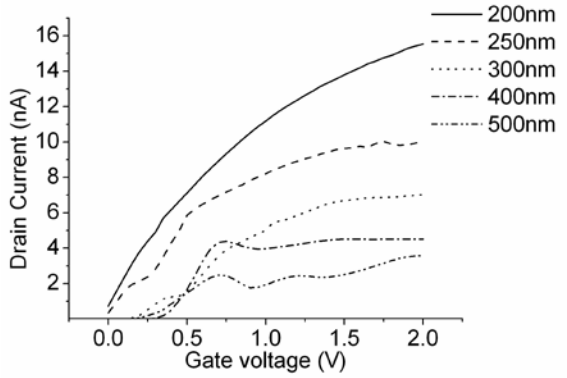


Fig. 3. $I_D$ - $V_G$ of fabricated devices with different lengths measured at room temperature. Coulomb blockade oscillation is more pronounced for longer SiNWs, which are subjected to larger tensile strain.

The origin of the SET has been attributed to the formation of a quantum dot along the SiNWs [8]. Quantum size effect leads to an increase in the bandgap of SiNW [13]: Experiment and simulation results both show bandgap increase to 1.5 eV for SiNW with 3 nm diameter [14]. Concurrently, there is a lowering of bandgap near the center of the SiNWs due to large tensile strain induced by the oxidation. The lowering is around 0.12 meV/MPa [15]. These two effects result in the formation of a quantum dot sandwiched between two potential barriers that act as tunneling barriers. SET are hence formed in a self-aligned manner.

It is postulated that the dependence of the Coulomb blockade oscillations on the SiNW length is related to the different tensile strains induced in these SiNWs. Based on micro-Raman spectroscopy measurements, it has been previously reported that the tensile strain induced in GAA SiNW due to thermal oxidation distributes non-uniformly along its length. It is largest in the centre and decreases towards both ends of the SiNW [9]. For SiNWs with different lengths but same width, the tensile strain at the center of each SiNW has also been found to be lower with decreasing SiNW length in several works [9, 16]. Similar GAA SiNW were fabricated through thermal oxidation in the study and measurement shows that tensile stress decrease from 2 GPa to 200 MPa for SiNW length decreasing from 50 μm to 5 μm [9]. For our devices with shorter SiNWs, there is less oxidation-induced strain and hence the bandgap near the center of the SiNWs do not lower as much as those devices with longer SiNW length. As a result, the tunneling barrier is effectively lowered and the devices increasingly operate in a normal MOSFET mode rather SET mode, and accounts for the smearing out of the oscillations with decreasing SiNW length. Therefore, it can be concluded that lower tensile strain tends to deteriorate Coulomb blockade oscillation in SiNW based SET. Oxidation-induced strain together with the quantum confinement in SiNWs result in the operation of SET.

## 4. Conclusions

In summary, we have observed prominent Coulomb oscillation in GAA SiNW MOSFETs fabricated with optical lithography at room temperature. The Coulomb oscillation is weakened for SiNWs of shorter length, attributed to the lowering of the tunneling barriers as a result of the reduced oxidation-induced tensile strain in the SiNWs. It is verified that the mechanism in forming SET in SiNW device is the combination of barrier lowing due to the strain, and the barrier increase due to quantum confinement in extremely small nanowire. This indicated that the length is a crucial design parameter in the design of SiNW based SETs.

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