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Circuit Implementation of InAs Nanowire FET

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1. Introduction

III/V semiconductor may contribute to a further optimization of CMOS circuits due to higher carrier mobility, higher speed, and higher power added efficiency. Due to wafer size and cost constrictions III/V semiconductors are not considered to replace Silicon but to extend the performance of Si-based circuits for specific applications. The need for high mobility materials for low bias, and high speed circuits makes InAs a highly recommend candidate for integration in Si-circuits.

The growth of III/V semiconductor on silicon substrates has been studied intensively, but due to the high lattice mismatch the obtained material quality was not sufficient for most applications. Nanowires are known to overcome lattice mismatch constrictions and high performance InAs nanowire transistors on Silicon (111) substrates are demonstrated [1]. In the cited case ultra high resolution electron beam lithography has been used for position control which limits cost-effective mass applications. In addition, a full compatibility to CMOS circuits in terms of substrate orientation and thermal budget is very difficult to achieve.

We propose a hybrid integration of InAs nanowires on a wide variety of substrates with a very low thermal budget (100 °C). The position control shall be done by dielectrophoresis [2, 3]. We report here on a cost-effective fabrication of single and multiple InAs nanowire metal-insulator field-effect transistor (NW-MISFET) and their implementation in basic circuits using field-assisted self assembly.

2. Experiments

The InAs nanowires were synthesized by MOVPE using the vapour-liquid-solid growth mode using colloidal Au seed particles [4]. After loading into the low-pressure MOVPE system, the samples were annealed at 620 °C in order to form an Au–In eutectic interface. After annealing, the temperature was ramped down to a growth temperature of T_g = 400 °C. The nanowire diameter was varied from 30 nm to 100 nm. This non-lithographic bottom up synthesis approach may be a candidate for high volume and extremely cost-effective production.

The wires are transferred to a host substrate for device fabrication and circuit implementation. The position control is provided using a pre-patterned electrode pair and dielectrophoresic forces. Dielectrophoresis describes the manipulation of neutral nanowires in a liquid medium using a non-uniform alternating current (AC) electric field. In such an electric field a dipole moment is induced in the nanowires due to charge separation along the nanowires [2]. Because of the dielectrophoretic force the nanowires align with the electric field, move in direction of increasing field strength and finally bridge the electrodes [3]. This process is called field-assisted self assembly (FASA) [5].

Fig. 1 shows a nanowire MISFET with two gate fingers fabricated by FASA. A coplanar contact pattern with small input and output leads has been used to suppress the pad capacitance. The huge source pads in Fig. 1a result in an improved input/output isolation. For low parasitic capacitances a high resistive Si-substrate with 4 µm SiO_2 isolation layer is used. This way the coupling capacitance C_{io} is reduced to 0.6 fF and the pad capacitance is reduced to 2.4 fF. An omega shaped top gate is employed for easier fabrication and heterogeneous integration while still maintaining an almost full surrounding of the wire.

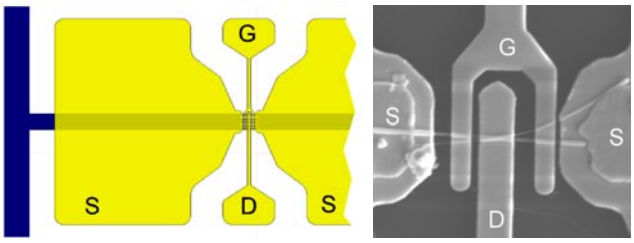

Figure 1: Nanowire MISFET: (a) FASA and coplanar contact pattern, (b) SEM micrograph of fabricated device.

The NW-FETs exhibit n-channel characteristics with very good saturation and a high output current for single as well as multi wire FETs. Typical on/off ratios of the drain current are about 1000. The maximum available gain of a multiple (in this case 7) nanowire MISFET with a gate length of L_G = 2×0,9 µm is reaches f_{MSG} = 7 GHz if deduced from measured scattering parameters. After deembedding of the parasitic environment discussed above the cut-off frequency surpassed 20 GHz.

Sample & Hold circuit

A Sample & Hold circuit (Fig. 2c) is a basic circuit often used in analogue to DC converters. The output V_{out} follows the input if the clk is high (sample phase). The output capacitor keeps the output fixed if the clk is low. This hold phase is needed to transfer the analog value to a digital one. In Fig. 2a,b the FASA method for heterogeneous integration of a sample & hold circuit is depicted. The fabrication starts with the patterning of the FASA electrodes (Fig. 2a).

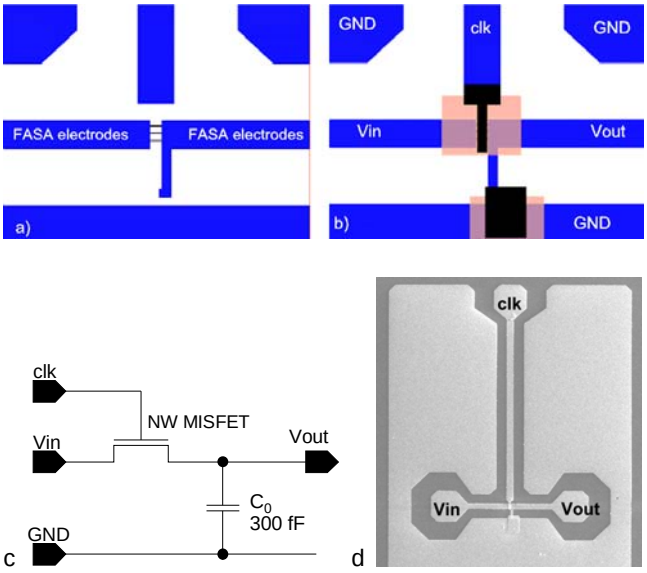

Figure 2: InAs nanowire Sample & Hold circuit: (a) layout for FASA electrodes used for nanowire deposition, (b) electrodes after SiNx and gate metal deposition, (c) schematics, (d) SEM micrograph of fabricated circuit.

Using dielectrophoretic forces the nanowires are deposited position controlled between these electrodes which are used as Vin and Vout terminals of the circuit. Next 30 nm SiN_x gate dielectric is deposited at room temperature. This layer is also used for the dielectric of the MIM hold capacitor C_0 which is fabricated on the ground metal (Fig. 2b). The process is finished with a Ti/Au top metallization for the gate and the interconnects..

The layout of the sample & hold circuit (Fig. 2d) is designed with coplanar GSG waveguides for an on-wafer characterization. The 50 Ohms characteristic impedance results in a short of the nanowire transistor output. Therefore Picoprode Model 35 active tips have been used for the measurement of the output signal V_{out}. The input impedance of these tips is as high as 1.2 MOhm and 0.5 pF.

2. Results

In Fig. 4 the transient behavior for an InAs nanowire sample & hold circuit with a clock frequency of 50 MHz is given. The sampling capacitor of 300 fF assures that despite the relatively high off current of the InAs transistor the output is kept constant in the hold phase (H) while the output signal still perfectly follows the input in the sample phase (S). The functionality of circuit was successfully tested up to a clock frequency of 1 GHz. At the beginning of each hold phase there is a 15 mV shift in the output voltage. Agilent Advanced Design System software was used to analyze this shift. The parameters of the EEMOS1 transistor device model were taken form experimental nanowire transistor data. The coplanar measurement environment including the active tips was also taken in to account. The simulated data (Fig. 3b) are in very good agreement with the experimental result. The measured shift is a result of the nanowire gate-source capacitance which results in a discharging of the hold capacitor and hence in the shift of the output.

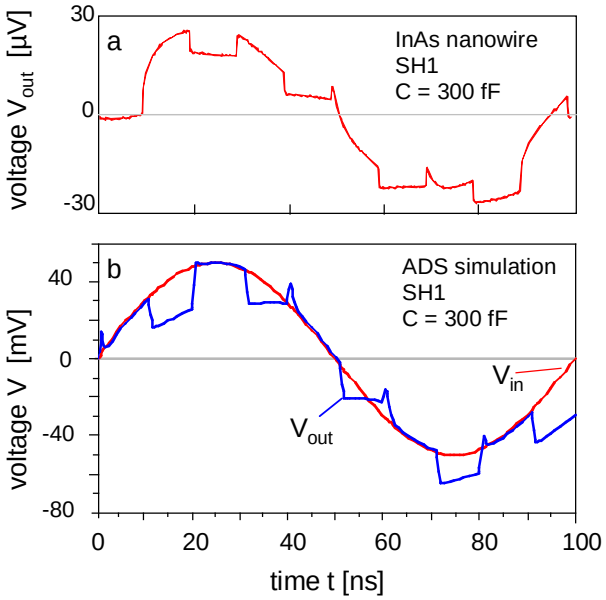

Figure 3: Transient behavior of an InAs nanowire sample & hold circuit at a clock frequency of 50 MHz: (a) experimental, (b) ADS simulation.

4. Conclusions

A heterogeneous integration of an InAs nanowire for the fabrication of a sample & hold circuit has been demonstrated. Due to the low thermal budget of 100 °C a wide variety substrates may be used for this process. Therefore, this process has a high potential for heterogeneous integration into advanced Si CMOS circuits. Moreover, flexible or organic substrates may also be used.

Acknowledgements

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