

Body-biased steep-subthreshold-swing MOS (BS-MOS) with small hysteresis, off current, and drain voltage

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Abstract

We demonstrate a 30-nm-gate-length nanowire MOSFET with steep subthreshold swing (SS). A parasitic bipolar transistor (PBT) formed in a fully depleted SOI MOSFET applies body bias (BB) to the MOSFET's channel and thus reduces the SS below 60 mV/dec at room temperature. Additionally, triple-gate operation allows current characteristics with small hysteresis, a high on/off ratio, and low drain voltage. These features promise SOI MOSFETs for low power consumption.

Introduction

The increase in performance of LSI circuits has been accompanied by continuously increasing power consumption. Among various origins of the increase in power consumption, the SS , whose minimum value is limited by operation temperature, gives rise to a fundamental limitation on power consumption reduction. To overcome such SS limitation, I-MOSs [1], tunnel FETs [2], and other type of FETs [3,4] have been studied. However, they each have various drawbacks, such as large drain voltage, large hysteresis in current characteristics, a small on/off current ratio, complicated device structures for a p-i-n channel and/or a gate, and mechanical instability, which lead to difficulty in their practical use. This report presents a BS-MOS with a nanowire channel, which overcomes these drawbacks.

Device fabrication and principle

A BS-MOS was fabricated on an SOI wafer. As shown in Fig. 1, the device has a wire channel and an upper gate (UG), lower gate (LG), and back gate (BG). Another structural feature of the BS is that it uses n^+-i-n^+ and p^+-i-p^+ channels for a n-type and p-type BS-MOS, respectively. Fig. 1(e) shows schematics of the n-type BS-MOS. The UG is used to invert the undoped channel so as to define source and drain regions electrically at both sides of the LG, which eliminates gate-induced-drain-leakage (GIDL) originating from pn junctions [5]. The LG turns the BS-MOS on and off like a conventional FET. Therefore, effective gate length corresponds to GL shown in Fig. 1(a). When drain voltage V_D is applied so that electron-hole pairs are generated by impact ionization near the electrically formed drain, holes flow to the body region of the SOI channel. Since such hole current gives forward bias to the source-body junction, which corresponds to the emitter-base junction of a PBT, drain current I_D is amplified by biased PBT, which leads to a smaller SS [6-8].

Demonstration

Fig. 2(a) shows I_D - V_{LG} characteristics of an n-type BS-MOS when V_D was changed. As V_D was increased, the SS became smaller at V_D higher than 2 V, and goes down to 6.6 mV/dec at V_D of 2.5 V [Fig. 2(b)]. Figs. 2(d)-(f) show contour plots of the minimum SS when V_{UG} and V_D were changed at various V_{BG} s. Larger V_{UG} and V_D allowed the BS-MOS to have SS smaller than 60 mV/dec [Figs. 2(d) and (f)]. The reasons for the small SS are that larger V_D increases the generation rate of impact ionization and that larger V_{UG} makes channel length shorter due to penetration of the electric field from the UG to the channel under the LG and thus increases the effect of the PBT [9]. Addi-

tionally, negative V_{BG} reduced the minimum V_D , at which SS was smaller than 60 mV/dec. This is because negative V_{BG} increases the number of holes accumulated at the bottom of the channel and thus enhances the effect of the PBT [the insets of Figs. 2(d)-(f)]. Therefore, optimization of V_{BG} is useful for low V_D operation. Note that relatively large V_{BG} does not lead to high power consumption due to constant V_{BG} .

Another noteworthy point is that off I_D is extremely small. This is because an electrical formation of the source and drain can eliminate pn junctions causing GIDL [5]. Since the PBT increases GIDL also [9], its fundamental elimination is essential for obtaining low off I_D .

Stable current characteristics are shown in Figs. 2(b) and (c): small hysteresis was obtained, compared to previously reported FETs with steep SS . In contrast, the BS-MOS with gate length of 60 nm had unstable current characteristics, i.e., large hysteresis and no controllability at larger V_D as shown in Fig. 3. Generally, shorter channel length enhances the PBT effect and thus leads to unstable characteristics [9]. The possible reason why our I-MOS shows the opposite behavior is that the longer channel leads to a larger body region, which increases in hole accumulation even when V_{BG} is 0 V, and thus to unstable current characteristics. Therefore, a smaller channel, which is, fortunately, a current trend in the MOSFET world, would be necessary to obtain stable current characteristics.

Finally, a p-type BS-MOS was demonstrated as shown in Fig. 4. The p-type BS-MOS also has current characteristics with small SS , hysteresis, and V_D . The possible reason why V_D at which the SS becomes steep in the p-type BS-MOS is higher than that in the n-type BS-MOS is that the rate of impact ionization caused by hole carriers is smaller than that caused by electron carriers. However, optimization of wire-channel structures and V_{BG} as in the n-type BS-MOSs would lead to further reduction in V_D even in the p-type BS-MOS.

In this report, since the intrinsic SS without the PBT effect, i.e., at small V_D , is larger than 60 mV/dec due to the relatively thick gate oxide, optimization of the device structure would improve the intrinsic SS , which promises further reduction of V_D to achieve steep SS .

Conclusion

We demonstrated BS-MOSs. A narrow and short channel fabricated on an SOI wafer leads to a small SS and makes drain voltage smaller. A two-layer gate allows small off current, i.e., a high on/off current ratio. These features bring BS-MOSs closer to practical use for achieving low power consumption.

References

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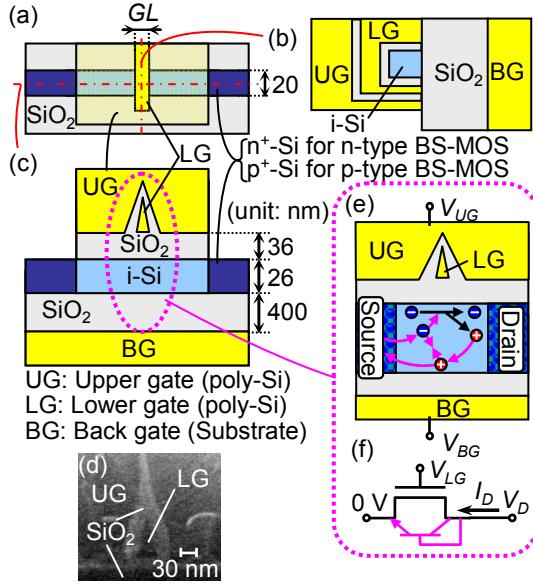


Fig. 1. Device structure of BS-MOSFETs. Schematic (a) top and (b-c) cross-sectional views along dash-dotted lines in (a). (d) SEM image of the cross-sectional view of the LG and UG formed on a SiO_2 substrate (not on the nanowire channel). (e) Schematics and (f) equivalent circuit of an n-type BS-MOS. To form a source and drain electrically, positive voltage is applied to the UG. The operation for a p-type BS-MOS can be achieved by applying voltage with opposite polarity to the device.

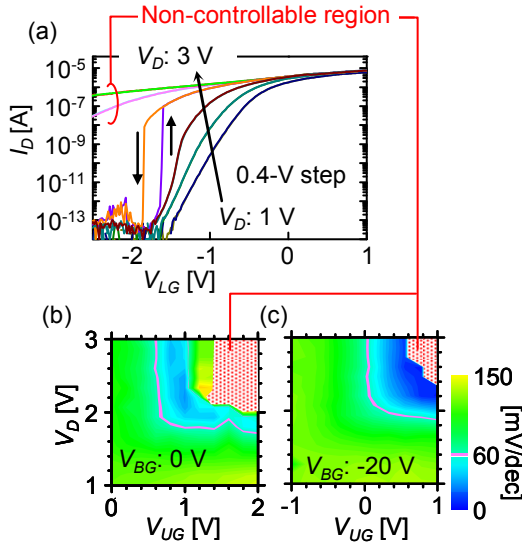


Fig. 3. Instability characteristics of the n-type BS-MOS with a longer channel (GL: 60 nm). (a) I_D - V_{LG} characteristics when V_{LG} was swept from -2.5 to 1 V and then returned to -2.5 V at various V_D s. (b)(c) Contour plots of minimum SS versus V_D and V_{UG} when V_{BG} was changed. The shaded areas mean poor controllability of current characteristics as shown in (a).

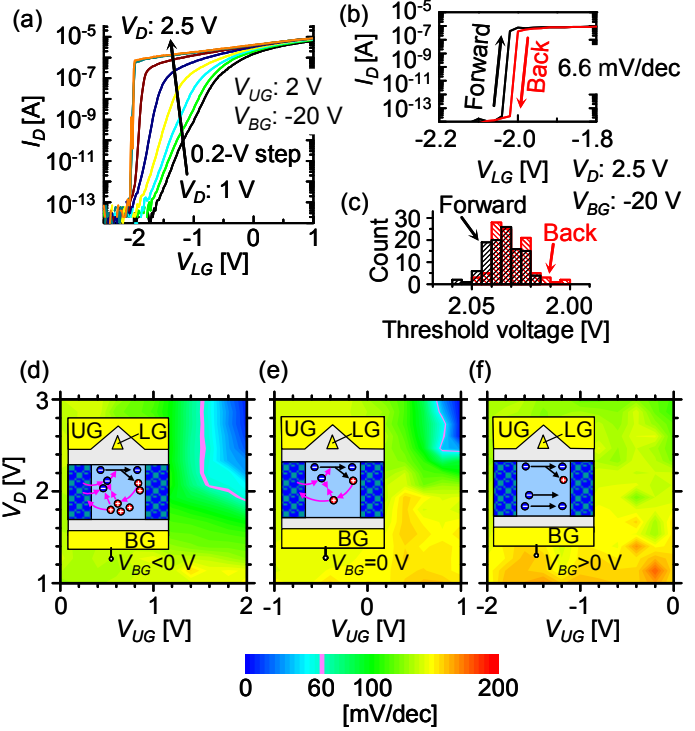


Fig. 2. Current characteristics of the n-type BS-MOS with W_{GL} of 30 nm. (a) I_D - V_{LG} characteristics when V_D was changed. (b) I_D - V_{LG} characteristics when V_{LG} was swept from -2.5 to 1 V and then returned to -2.5 V. (c) Histogram of threshold voltage at which I_D was 10^{-10} A. In (b) and (c), V_{BG} and V_D were -20 and 2.5 V, respectively. Contour plots of the minimum SS versus V_D and V_{UG} when V_{BG} was (d) -20, (e) 0, and (f) 20 V. The insets show schematics of the effect of the parasitic bipolar transistor. When V_{BG} is positive, electron channels are formed at the top and bottom of the wire channel.

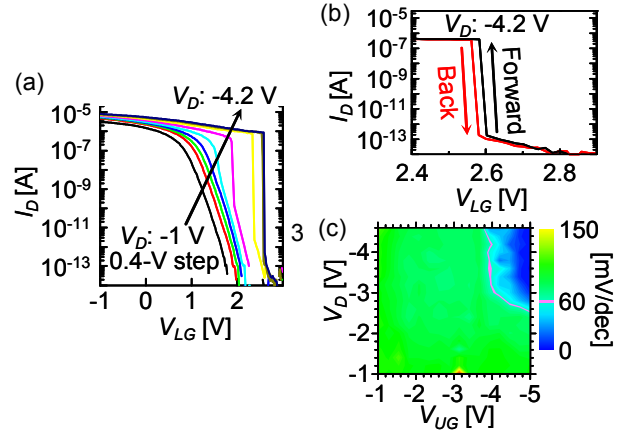


Fig. 4. Current characteristics of a p-type BS-MOS with GL of 30 nm, respectively. The differences between the n-type and p-type BS-MOSs are the heavily doped channel as shown in Fig. 1(b) and the polarity of voltages applied to the LG and UG. (a) I_D - V_{LG} characteristics when V_D was changed. V_{BG} was -20 V. (b) I_D - V_{LG} characteristics when V_{LG} was swept from 3 to -1 V and then returned to 3 V. (c) Contour plots of minimum SS versus V_D and V_{UG} when V_{BG} was -20 V.