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Impacts of Diameter-Dependent Annealing in Silicon Nanowire MOSFETs

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Abstract

In this paper, an abnormal diameter-dependent annealing (DDA) effect in silicon nanowire MOSFETs (SNWTs) is reported and investigated for the first time. It is found that the implanted dopants diffuse faster in thin nanowires than those in thick nanowires during annealing process, which results in underestimating the length of designed S/D extension region in SNWTs. The impacts of DDA on SNWTs are studied in terms of S/D resistance, threshold voltage shift, tradeoff between parasitic capacitance and resistance. The impacts of different implantation and annealing conditions are also discussed.

Introduction

Recently, the silicon nanowire MOSFET (SNWT) with gate-all-around structure has attracted much attention due to its excellent electrostatics and improved transport [1-4]. On the other hand, the source/drain (S/D) series resistance (R_{sd}) and parasitic capacitance play an important role in SNWTs due to the unique structural nature of ultra-narrow nanowires. Thus, the S/D extension region is a major design concern for SNWTs. The doping profile optimization [5] and impacts of random dopant fluctuation [6] in these regions have been reported. However, the fabrication process dependence of the doping in S/D extension regions has not been studied. Therefore, in this paper, the S/D dopant activation process in SNWTs is investigated, in which an abnormal diameter-dependent annealing effect is observed and discussed.

Simulation Method

The implant and annealing processes are simulated by 3-D atomistic kinetic Monte Carlo method [7]. Arsenic are implanted only in the large S/D region at 0^o angle with the expected concentration peak close to the intrinsic nanowire channel, then the annealing is performed at 1050^oC, 2 ms so that the dopants diffuse into the nanowire. Fig. 1 shows a typical process result, in which the discrete impurities and defects are distributed in both large S/D and S/D extension regions of nanowire. Then the discrete dopants are converted to continuous doping profile, which is as the input of the following 3-D device simulations. The gate length (L_g) of simulated SNWTs is 40nm, the gate spacer length (L_{spacer}) is 20nm, gate height is 80nm and the nanowire diameter (d_{NW}) is within a variety range from 4nm to 44nm.

Results and Discussion

Fig. 2 shows the total resistance (normalized to the cross-section area of nanowires) of the simulated devices with different nanowire diameters. For each diameter, 50 samples are implanted and annealed. The results indicate that the total resistance (R_{total}) of processed SNWTs decreases with nanowire diameter scaling and would saturate at extremely thin nanowire. This can be explained by Fig. 3 that the dopants diffuse faster in thinner nanowires, which is probably due to the reduced diffuse barrier and enhanced effective source concentration in narrower nanowires. Fig. 4 further plots the extracted effective length of extension regions (L_{ext}) and the portion of parasitic R_{sd} over R_{total} with different diameters. The L_{ext} in 12nm-diameter SNWTs is twice of that in 44nm SNWTs, with the same L_g and same process conditions. It is also worth noting the variation of R_{total} due to the fluctuation of DDA. Since dopants diffuse faster in thinner nanowires, it will in turn have more variations, as shown in Fig. 2, until the saturation in extremely thin nanowires.

Fig. 5 shows the median I_{ds}-V_{gs} characteristics of SNWTs with different diameters. Fig. 6 further compares the threshold voltage (V_{th}) shift with and without the DDA effects, which indicates that DDA has significant impacts on the V_{th} design of SNWTs. Fig. 7 compares the different impacts of DDA on the parasitic resistance and capacitance in SNWTs. On the contrary to parasitic resistance, the parasitic capacitance component increases with nanowire diameter scaling; and the change magnitude of the capacitance is larger than the change of resistance, which indicates that the DDA has more influence on parasitic capacitance than the series resistance.

Fig. 8 also discusses the impacts of different process conditions. Higher annealing temperature could result in larger L_{ext}, however, the total resistance is almost unchanged as shown in Fig. 8 (a), which indicates the potential of low-temperature annealing for S/D activation in SNWTs. In addition, the total resistance also not very sensitive to implant energies, except the concentration peak is far away from the nanowire (for too low energy), as shown in Fig. 8 (b).

Summary

In this paper, an abnormal diameter-dependent annealing (DDA) effect in SNWTs is investigated for the first time. It is found that the implanted dopants diffuse faster in thinner nanowires during annealing process. The impacts of DDA on the S/D resistance, V_{th} shift, and parasitic capacitance in SNWTs are studied, providing some design tradeoffs on the S/D extension regions in SNWTs. The impacts of different implant and annealing conditions are also discussed.

Acknowledgement

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References: [1] S.D. Suk *et al.*, *IEDM*, p. 717, 2005; [2] N. Singh *et al.*, *IEDM*, p. 547, 2006; [3] Y. Tian *et al.*, *IEDM*, p. 895, 2007; [4] T. Ernst *et al.*, *IEDM*, p. 745, 2008; [5] J. Zhuge *el al.*, *IEEE T-ED*, vol. 55, no. 8, p. 2142, 2008; [6] N. Seoane *el al.*, *IEEE T-ED*, vol. 56, no. 7, p. 1388, 2009; [7] Sentaurus TCAD tools.

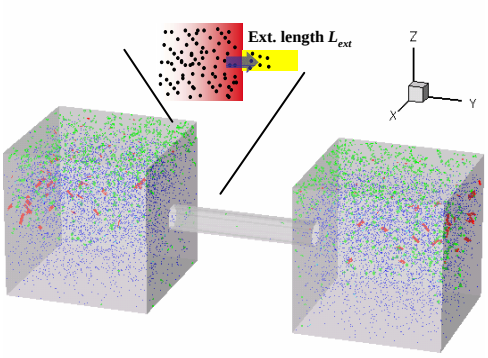

Fig. 1 The typical results of simulated SNWTs after the implantation and annealing. The blue dots present for impurities, red dots and green dots present for defects.

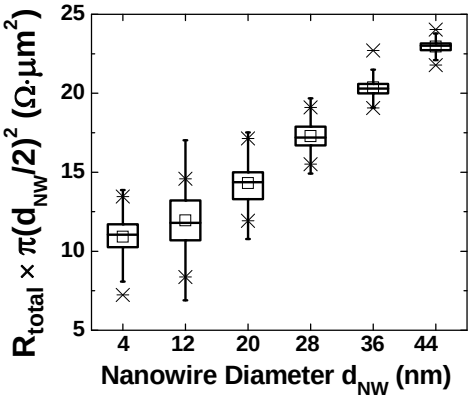

Fig. 2 The normalized total resistance of SNWTs with varying nanowire diameters.

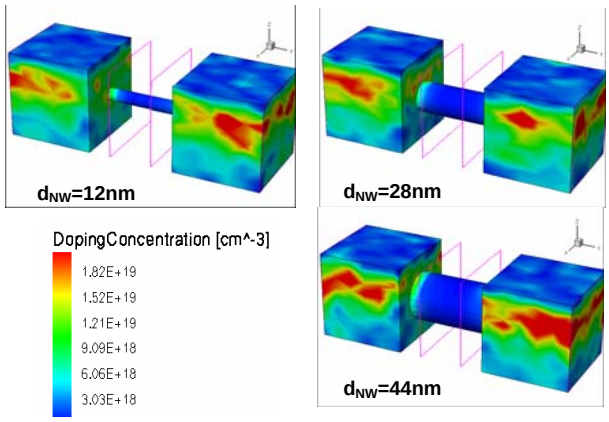

Fig. 3 Examples of doping concentration in SNWTs with different nanowire diameters. The sample devices are taken from the median total resistance results.

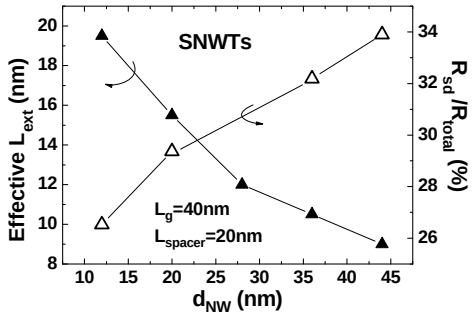

Fig. 4 The extracted median effective length of S/D extension region (L_{ext}) and the portion of parasitic R_{sd} over R_{total} as functions of nanowire diameters.

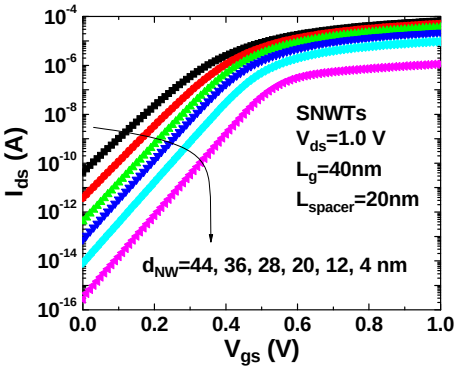

Fig. 5 The median transfer characteristics of simulated SNWTs with different diameters, which shows large impacts of the diameter-dependent annealing effects.

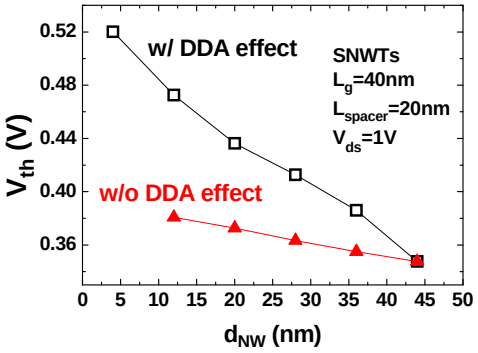

Fig. 6 Impacts of DDA effect on the threshold voltage shift of SNWTs with nanowire diameter scaling. The threshold voltages are of their median values

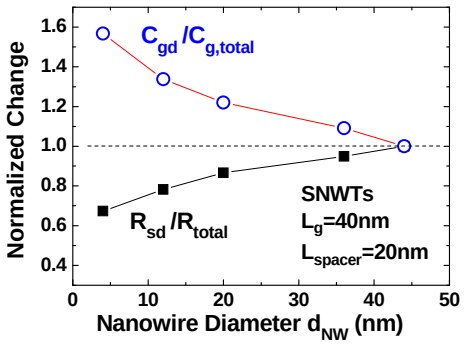

Fig. 7 The impacts of DDA effects on the parasitic S/D resistance and capacitance in SNWTs. The parameters are of their median values.

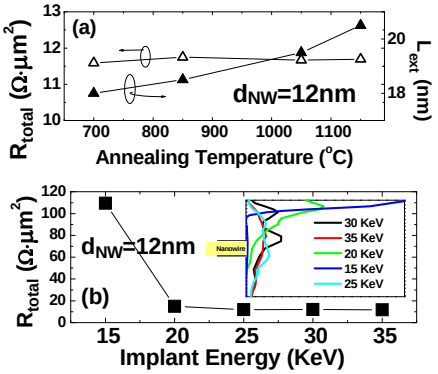

Fig. 8 The impacts of different annealing temperature (a) and different implant energy (b) on the DDA effects in SNWTs. The parameters are of their median values. The inserted is the doping profile in the large S/D region with different implant energy.