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# Electrical Characterization of InGaAs nanowire MISFETs Fabricated by Dielectric-first Process

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## 1. Introduction

Epitaxially grown semiconductor nanowires (NWs) have attracted much attention for their unique electrical and optical properties for future device applications, such as in field effect transistors (FETs), laser diodes, photovoltaic devices, and so on. For instance, free-standing vertical surrounding gate (VSG) FETs are demonstrated by several groups [1,2], in which excellent gate controllability and effective suppression of short channel effects are expected. To date, most NWs have been formed by catalyst-assisted vapor-liquid- solid (VLS) growth mechanism. However, the precise site control of NWs is difficult unless conventional lithographic techniques as defining the position of nanoparticle catalyst. Furthermore, it is thought that incorporation of catalyst into NWs deteriorates the crystalline quality.

We have already reported on an alternative method, that is, catalyst-free selective-area metal-organic vapor phase epitaxy (SA-MOVPE) [3,4] for forming NWs. This method is capable of growing NWs at adequately predetermined positions without any aids of catalysts. We have demonstrated characterization of InAs NW-VSGFETs on Si substrate and exhibited excellent properties [5]. However, the structures of VSGFETs are extremely complicated and it is not easy to perform basic characterizations. In this sense, lateral NW-FETs [6,7], which is easier to fabricate, are more adequate for electrical measurements of single NWs to study and to demonstrate their intrinsic performance. Also, we have already reported on the fabrication and electrical characterization of *n*-type InGaAs Schottky top-gate NW-FET [8]. However, sufficiently good output characteristic with reasonable reproducibility and, furthermore, top-gate metal-insulator-semiconductor (MIS) FETs has not demonstrated yet.

In this paper, we attempted gate-dielectric-first process for the back-gate and top-gate intentionally doped InGaAs NW-MISFETs. By introducing this process, drain current of FETs was improved greatly as compared to those fabricated using conventional process.

## 2. Experimental Procedures

*2-1. SA-MOVPE growth of InGaAs NWs*

InGaAs NWs were grown by the following procedure. First, after the deposition 20nm-thick $SiO_2$ film on InP (111)B substrates by RF sputtering, an array of holes with diameter of about 250 nm was defined on $SiO_2$ masked substrate by electron-beam (EB) lithography and wet etching. Then, InGaAs NWs were formed on the partially masked substrate in the low-pressure horizontal-MOVPE system, supplying trimethylindium (TMIn), trimethyl-gallium (TMGa), and 5% arsine ($AsH_3$) diluted in $H_2$ as source materials. The partial pressures of TMIn, TMGa, and $AsH_3$ were $9.15\times10^{-7}$ atm, $5.68\times10^{-7}$ atm, $6.0\times10^{-4}$ atm, respectively. The growth temperature for InGaAs NWs was 650℃. With these conditions, free-standing NWs with hexagonal cross sections were formed selectively in the circular opening area of the mask. A scanning electron microscope (SEM) image of InGaAs NWs is shown Fig.1. The growth time was 70 min. The length of each NW was 10μm, and their diameters were 250 nm. The alloy content In for InGaAs NWs was estimated to be 35% from X-ray diffraction measurements.

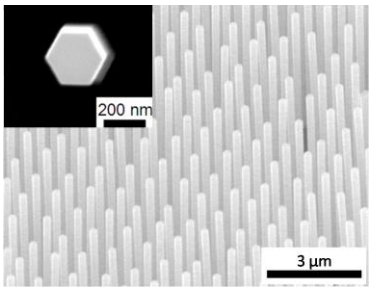


**Fig. 1 :** SEM images of InGaAs NWs fabricated by SA-MOVPE.

*2-2. Device fabrication process*

Schematic of InGaAs top-gate NW-MISFETs with single NWs is shown in Fig. 2. Gate dielectric of $Al_2O_3$ was formed to cover all the periphery of NWs by depositing $Al_2O_3$ on free-standing NWs. Fabrication procedure is as follows. First, after a removal the native oxide by wet etching using alkali solution, whole surface and NWs were covered with $Al_2O_3$ formed by atomic-layer-deposition as high-*k* gate dielectric. The thickness of $Al_2O_3$ was 10nm. Then, the NWs were removed from growth substrates and dispersed in ethanol by sonication and then transferred to a *p*+ Si substrate with 200nm-thick $SiO_2$ overlayer. A conductive substrate was used as a back gate. Area for ohmic contacts was defined by EB lithography, followed by the removal of $Al_2O_3$ using wet etching in buffered HF (BHF, $NH_4F$:HF =5:1). Subsequently, metals (Ti/Al/Ti/Au= 20/170/10/50nm) on the source and drain contacts were formed by EB evaporation and lift-off technique. The length between source and drain was designed to be 1 or

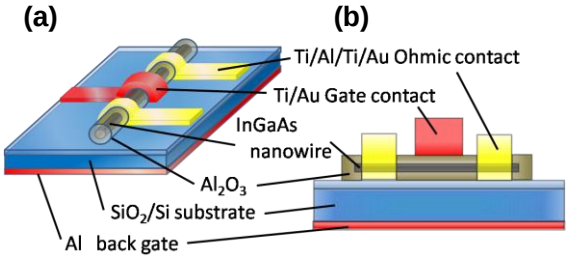


**Fig. 2:** Schematic of (a)InGaAs NW top-gate MISFET structure and (b) its cross-sectional view.

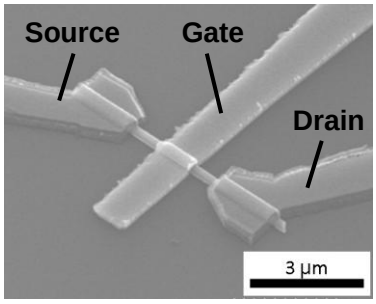


**Fig. 3:** SEM image of InGaAs top-gate NW-MISFET.

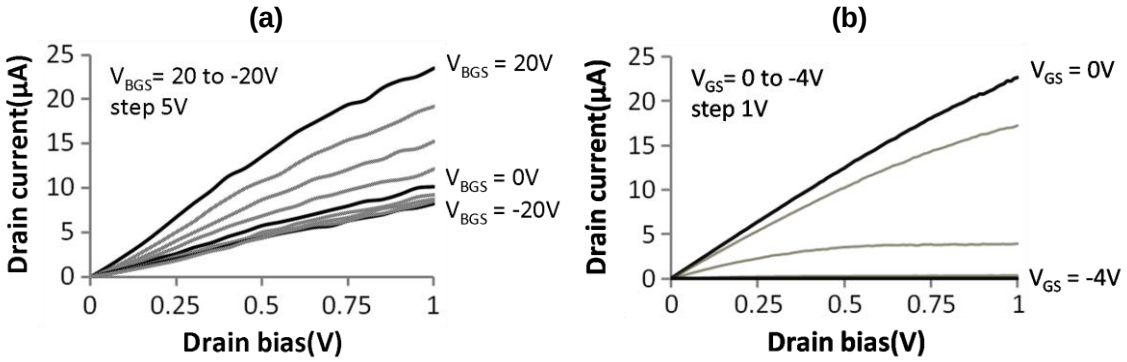


**Fig. 4:**(a) Drain characteristics of InGaAs NW back-gate MISFET ($V_{BGS}$= +20V to -20V in 5V step, @RT).
(b) Drain characteristics of InGaAs NW top-gate MISFET ($V_{GS}$= 0V to -4V in 1V step, @RT).

3µm. Finally, top gate metals (Ti/Au=30/230nm) were formed by EB lithography, EB evaporation, and lift-off technique. No thermal treatment was performed prior to or after the gate formation. A SEM image of top-gate MISFET is shown Fig. 3. The gate length was 1µm and the spacing between source and drain was 3µm.

Electrical characteristics of back-gate and top-gate MISFETs measured by using parameter analyzer (Agilent_ 4156) at room temperature.

### 3. Results and discussions

Figure 4(a) shows drain characteristics of an InGaAs back-gate NW-MISFET without a top gate. The distance between source and drain, i.e., effective gate length was 1µm. NW-MISFET exhibited *n*-type characteristics, as expected. FETs did not turn off completely, probably due to bad capacitive coupling between NW channel and back gate and to leakage current. It is noted that the drain current density (per unit NW diameter) is comparable to devices using *n*-InGaAs NWs reported previously [8], at drain bias $V_{DS}$=1V and back-gate bias $V_{BGS}$=0V. Furthermore, maximum drain current is much larger than the previous report when back-gate voltage is positively biased. These results are promising for FETs if one considers that the present NWs are unintentionally ones.

Next, we measured the characteristics of top-gate NW-MISFET. Results are shown in Fig. 4(b). We obtained good saturation characteristics, turn-off behavior, and drain current density of 95mA/mm at $V_{DS}$=1V and top-gate bias $V_{GS}$=0V. This value is much larger than those obtained in our previous *n*-InGaAs NW MESFETs, and is comparable to those in InAs NW- VSGFET with gate length of 300nm [5].

We think this improvement in drain current is due to the improvement of the property of dielectric-NW interface. That is, by depositing $Al_2O_3$ just after the chemically treated NW surfaces, interfacial disorders or impurities which lead to the interface states was reduced. Although we still need further optimization of the NW size and the processing for devices, present gate-dielectric-first process is promising to improve characteristics of NW-FETs. This approach will also be useful to investigate and optimize interfacial properties between NW and dielectrics, because it is possible to systematically perform surface treatment for a bunch of NWs.

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