Multi-fingered LDMOS thermal analysis based on a distributed thermal network

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1. Introduction

Self-Heating Effect (SHE) is commonly responsible in performance degradation for high voltage MOSFETs [1]. Large impact is observed on huge multi-fingered devices, which are used in power management or power amplifier applications. Distributed thermal network have been used to model SHE [2] [3]. So far, studies mainly focused on the total thermal resistance (Rth) of the multi-fingered device. In this paper, we present a distributed thermal network tool named GenSHE, allowing to have an accuracy insight into the thermal coupling of multi-fingered devices. Simulation results have been compared with experimental data on recently developed test structures [4] [5].

2. Distributed thermal network

A distributed thermal network approach can be used to describe both the heat propagation within structures and the interaction between the different heat sources. Heat dissipation is represented by resistances, which describe geometric regions traversed by the heat flow. Some assumptions have been made in the calculation: The heat dissipates in two directions: through Si substrate and through back-end metallization. Trench isolation (shallow trench isolation, STI and Deep Trench Isolation, DTI) are considered to behave as a perfect heat isulator. The heat source has the dimensions of gate finger. The heat flow is supposed to be confined within a 45° pyramid based on the channel (Fig.1). The structure NLDMMOS can be divided into different regions: 3D Pyramid at sources of heat, Semi-3D Pyramid when flows from two sources are in contact, 2D Pyramid when the STI limit the flow, 2D Pyramid deep in the substrate, 2D Pyramid for coupling between the sources. From physically simulation and previous works [2] [3], a thermal resistance network has been calculated from the layout (Fig.2) by solving the equation (1):

$$R_{th} = \rho \int_{W(z)}^{L(z)} z \int_{L(z)}^{W(z)} dz$$

GenSHE receives as input geometric and technology parameters (Fig.3). The thermal network has been generated from several sources (pair of fingers) of NLDMMOS, and implemented on the commercial circuit simulator, using the compact model (BSIM3SOI). The thermal network replaces the internal thermal resistances of compact model. Consequently, the transistors are not only connected by electrical nodes, but also by thermal nodes.

3. Experimental results

The NLDMMOS transistor investigated in this work has been integrated using 250nm CMOS process (Fig.4): polysilicon gate length is 0.5 µm, N+ drain extension length is 0.6 µm, and gate oxide thickness is 5nm. The off-state breakdown voltage is larger than 15V and S.Ron is 12 mΩ.mm². The device operates with gate voltages up to 2.5V.

Using GenSHE, intrinsic Rth is given for each source (Fig.5). Switching on only one source, GenSHE accurately predicts the isolation impact: intrinsic Rth increases for sources closer to the active edges as temperature dissipation is reduced near the STI. This behavior is also confirmed with silicon measurements on an NLDMMOS with Nsource=5 (Fig.6). The simulation confirmed the need to take into account the heat flow through the metallization in order to be sufficiently accurate. When all sources are switched-on at the same time (Fig.8, b) the temperature and the equivalent thermal rises due to the thermal coupling effect. The thermal coupling between sources is the dominant effect: thermal resistance and temperature is maximal on sources in the center of the device. Considering large multi-sources devices, in the case of sources in central position (Fig.7, a), we observed that the coupling coefficient [4] between two adjacent sources is the same whatever the sources number. If we considered the second neighbour instead of the first one, the coupling coefficient is reduced by a factor 2; we also observe that the coupling effect decreases, when the spacing between the sources increases. GenSHE simulations confirm previous SHE models presented in [5]. In addition, a good agreement is observed when comparing simulation with silicon measurements on coupling coefficient, and global Rth profile (Fig.6, Fig.7, b) and (Fig.8, b). Results demonstrate that GenSHE simulations well predict the thermal behavior of the device whatever the number and the position of the switched on sources.

3. Conclusion

The proposed thermal resistances network GenSHE predicts both self-heating and thermal coupling effects in NLDMMOS, regardless of its geometry.

The ability of GenSHE to reproduce the thermal characteristics of multi-fingered NLDMMOS devices has been demonstrated. The approach of GenSHE has the advantage of being independent of thermal resistance extraction on electrical measurement. These results are highly promising for modeling thermal effects in power transistor.
References


Fig.1: Simplified representation of transistors heat flow and the associated thermal resistances

Fig.2: Expression for the calculation of thermal resistance as a function of geometry

Fig.3: Input parameters of GenSHE: geometry and technology

Fig.4: Cross-sectional view of an NLDMS

Fig.5: Simulated intrinsic thermal resistance for devices with different Nsource, Wactwve=10µm.

Fig.6: Comparison between measured and simulated intrinsic thermal resistance for NLDMS with 5 sources.

Fig.7: a) Coupling coefficients extracted for NLDMS with 10 sources. 
   b) Comparison between measured and simulated coupling coefficients C1n.

Fig.8.a) Simulated thermal resistance for devices with different Nsource. b) Comparison between measured and simulated thermal resistance profile for NLDMS with 5 sources.