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Invited Paper

Recent Progress in High Voltage MOS-gated Power Transistors in GaN

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GaN is attractive for high-temperature and high-voltage power devices because of its wide bandgap (3.4 eV) and high critical electric field (3 MV/cm). In addition, thin GaN layers can be heteroepitaxially grown on large-diameter sapphire and silicon substrates, allowing the use of Si CMOS foundries for cost-effective device processing. While lateral Schottky-gate HEMTs with AlGaN/GaN heterojunction channel and drift regions have been widely explored [1], MOS channel in GaN transistors have shown to exhibit low gate leakage current, enhancement mode operation with a large positive threshold voltage, and Si CMOS-compatible processes [2-8].

In this paper, we review the progress in the development of high-voltage MOS-gated power switching FETs in GaN. We present the advantages and disadvantages of various device structures explored. In addition, we will discuss technology issues such as surface passivation and reliability issues such as current collapse. Further, we will present the future trend and the competitiveness of GaN vs. SiC for power electronics.

Vertical device structures are more area efficient but native GaN substrates are still very expensive. By contrast, lateral device structures can be implemented on large-diameter silicon substrates but the wafer bowness and defect density still need to be controlled. Besides the conventional HEMTs and MOSFETs, MOS-gated HEMTs integrates a normally-off MOS channel with a highly conductive AlGaN/GaN heterojunction drift region, which supports high voltages with polarization charges inherent in the heterojunction.

Several lateral MOS-gated power transistors in GaN have been experimentally demonstrated. Lateral RESURF GaN MOSFETs have been realized with either implanted or epi drift region. Implanted devices with BV as high as 2.5kV has been implemented but the dosage control of the activated dopants in the drift region is difficult [5]. Epi-RESURF MOSFETs with BV of 730V and $R_{on,sp}$ of 34mΩ-cm^2 have also been demonstrated [6]. In addition, several MOS-gated HEMTs have been reported, increasingly scaled to shorter channel lengths, because of the dominance of the channel component of the on-resistance due to a lower (at least 10-100x) channel mobility vs. 2DEG mobility [9], resulting in $R_{on,sp}$ of 4.2mΩ-cm^2 and BV of 643V [10]. Further, gate oxide breakdown at gate corner near drain side needs to be avoided in MOS-gated HEMTs by optimizing net polarization charges and field shielding with surface field plated and underlying p regions. The highest BV experimentally achieved for MOS-HEMTs is 1300V [7].

Because the insulating sapphire substrate cannot provide negative charges, other ways to achieve good dielectrically isolated (DI) RESURF are worth investigating, such as balancing the positive polarization charges to negative polarization charges at another GaN/AlGaN interface. Another approach is to use GaN on silicon substrate, where the conducting substrate can provide negative charges for terminating field lines and a more uniform field distribution, similar to the RESURF action in silicon-on-insulator (SOI).

When compared to SiC, GaN power switching transistors offer a low-cost, large-diameter silicon substrate with Si CMOS foundry compatibility, though at a lower (2-3x) area efficiency due to lateral device structures, and hence are expected to be competitive for blocking voltage ranges 2kV or below.

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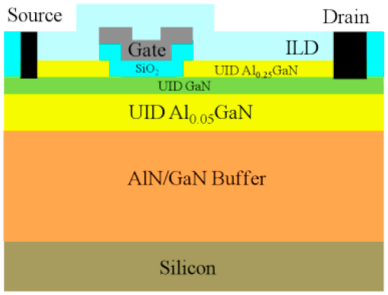

Fig. 1 Schematic cross-section of lateral hybrid MOS-gated HEMT on silicon substrate

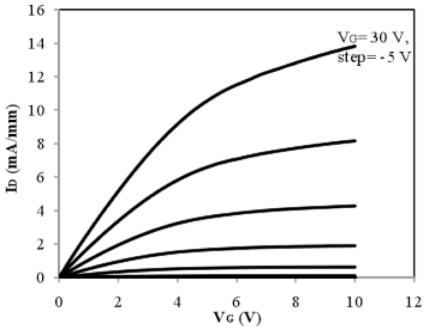

Fig. 2 Output I-V characteristics of MOS-gated HEMT with 3μm channel length and 24μm RESURF length on silicon substrate

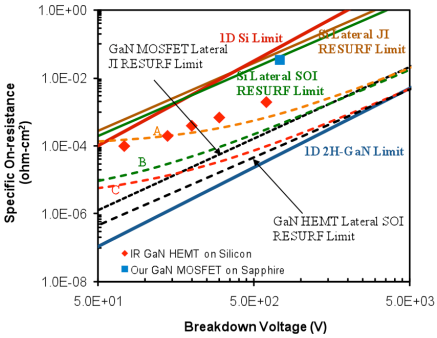

Fig. 3 Breakdown voltage vs. specific on-resistance trade-off for GaN MOSFETs and MOS-HEMTs, along with material limits

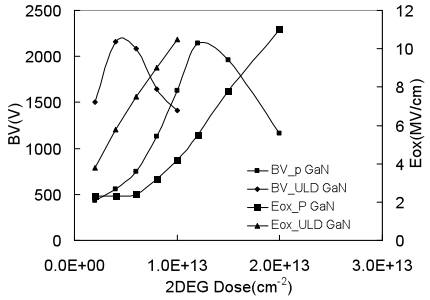

Fig. 4 BV and oxide electric field for different 2DEG sheet carrier density with 4μm channel length and 20μm drift length (V_{DS}=1200V or BV) on 3μm ULD GaN and P-GaN ($3\times10^{16}cm^{-3}$)

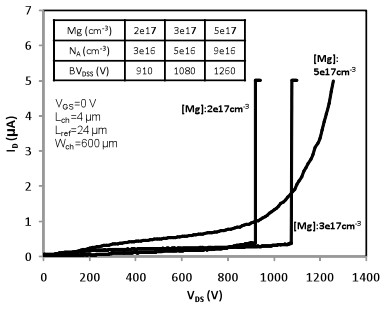

Fig. 5 Blocking I-V characteristics of GaN hybrid MOS-HEMT with different Mg contents and RESURF length of 24 μm

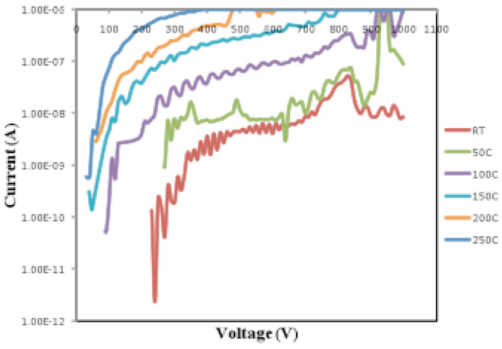

Fig. 6 Blocking I-V characteristics of lateral GaN epi test structures on silicon substrate at various temperatures