Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp1303-1304

Fabrication of defect-free and relaxed Ge-rich SGOI-wire structures for CMOS applications

Minoru Oda, Yoshihiko Moriyama, Keiji Ikeda, Yuuichi Kamimuta, and Tsutomu Tezuka
MIRAI-Toshiba, 1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki, 212-8582, Japan,
Phone : +81-44-549-2313, Fax: +81-44-520-1257, E-mail : minoru2.oda@toshiba.co.jp

Introduction

Strained SiGe with a high Ge fraction has been known to exhibit high electron and hole mobility under tensile and compressive strain, respectively [1]. On the other hand, non-planar MOSFET structures such as FinFET or gate-all-around FET are expected to have strong immunity against short-channel effects [2]. Therefore, non-planar MOSFETs with strained Ge-rich SiGe or Ge channels are very promising for high-performance CMOS devices that have high drive current and low off-leakage current. A significant increase in drive current has already been demonstrated in a compressively strained SiGe-on-insulator (SGOI)-wire p-MOSFET [3] fabricated by the Ge condensation technique [4]. On the other hand, the compressive strain is inappropriate for SGOI-nMOSFETs [1]. Since SGOI channels formed by the Ge condensation technique have compressive strain [5] or are relaxed with introducing crystalline defects [4, 6], the compressive strain should be released without introducing them for n-MOSFETs. Recently, T. Tanaka et al. showed how to produce a high-quality SGOI layer by rapid melting growth [7], using Si substrate as a seed region. In this paper, we propose a novel process to form strain-relaxed and defect-free Ge rich SGOI-wire structures as templates for non-planar strained SGOI CMOSFETs without the additional Si substrate seed regions.

Concept of condensation-melting-recrystallization process

Fig. 1 shows the concept of the new fabrication process. First, a SGOI wafer formed by the Ge condensation technique [4], is patterned into mesa structures consisting of a narrower channel and a wider source region as shown in Fig. 1(a). The SGOI mesas are then thermally oxidized to enrich the Ge content [8]. During the oxidation, a Ge fraction, x, becomes higher in the narrower region than in the wider region owing to the oxidation on the sidewalls in addition to the oxidation on the top surface. As a result, the SGOI channel (narrower region) has higher x than the source region (wider region) as shown in Fig. 1(b). The wafer is annealed at a temperature higher than the melting point of SiGe in the channel but lower than that in the source region, then the wafer is cooled down. As the temperature decreases, the molten channel recrystallizes from the source region as a seed region and the initial compressive strain is released as shown in Fig. 1(c). Fig. 1(d) shows a final CMOS device having stressors to produce compressive and tensile strain in the p- and n-channels, respectively.

Experimental

A SGOI(x = 0.08) wafer was formed after the Ge condensation process from an epitaxial wafer of 56-nm $Si_{0.9}Ge_{0.1}$ on SOI wafer. A thermal oxidation process was carried out at 900 ^{o}C for the second Ge condensation of SGOI mesas, which were patterned by electron-beam lithography followed by an RIE process. The oxidation was stopped when the Ge fraction of the channel with a width of 20 nm and the wider source had become about 0.9 and 0.45, respectively. The wafer was annealed in N_2 atmosphere at a peak temperature of 1090 ^{o}C, at which only the channels melted. After cooling down, the SGOI mesas before and after the annealing were analyzed by plan-view and cross-sectional TEM measurements to assess the crystallinity and crystalline defects. The Ge fraction and the strain were evaluated by TEM-EDX and Raman spectroscopy measurements, respectively. The Raman spectroscopy was also employed to determine both Ge fraction and the strain nondestructively during the process [9].

Results and discussion

The Ge profile in the SGOI mesa (Fig.2) observed by a HAADF-STEM measurement after the second condensation process exhibits a bright contrast, i.e., higher Ge fraction, in the channel region and the periphery of the source region. The recrystallization after the melting process is considered to initiate from the central region of the source indicated as the darker area in Fig. 2. Fig. 3 and Fig. 4 show plan-view and cross-sectional TEM images of the middle of the channel region after recrystallization. No crystalline defects such as dislocations or planar defects were found from the TEM images of the channel region. Electron-beam diffraction patterns in Fig. 5 indicate that the crystalline orientation is same as that of the source.

The TEM-EDX measurements (Fig. 6) revealed that the Ge fraction was uniform across the channel and amounted to 0.92 and 0.79 before and after the melting and recrystallization processes, respectively. The slight decrease in the Ge fraction after the recrystallization may be caused by out-diffusion of Ge from the SiGe channel to the oxide covering the channel. Fig. 7 and Table 1 show the strain relaxation in the channel from 3.6% compressive (if uniaxial strain is assumed [9, 10]) to almost zero after the melting and recrystallization processes. These results indicate that the strain-relaxed and defect-free SGOI wire structures were realized by the present process.

Conclusion

Strain-relaxed and defect-free SGOI wire structures were demonstrated by the proposed condensation-melting-recrystallization process. This technique will enable us to fabricate non-planar Ge-rich SGOI CMOS devices with additional stressor techniques for high-performance or low-power consumption applications.

Acknowledgements: This work was supported by NEDO. The authors are grateful to Dr. T. Horikawa and technical staff in AIST-NIRC for their support in the lithography and RIE processes.

References

[1] M. V. Fischetti et al., J. Appl. Phys. **80**, 2234 (1996)
[2] Jean-Pierre Colinge, Solid-State Electronics, **48**, 897, (2004)
[3] T.Irisawa et al., IEEE Trans. Electron Devices, **53**, 2809 (2006)

[4] T. Tezuka et al., Jpn. J. Appl. Phys., **40**, 2866 (2001)
[5] T. Tezuka et al., Appl. Phys. Lett., **94**, 081910 _2009
[6] S. Nakaharai et al., Semicond. Sci. Technol. **22,** 103 (2007)
[7]T. Tanaka et al., Appl. Phys. Express **3**, 031301(2010)
[8] T. Irisawa et al., Thin Solid Films., **517**, 167 (2008)
[9] J. C. Tsang et al., J. Appl. Phys. **75**, 8098 (1994)
[10] T. Ito et al., Jpn. J. Appl. Phys., **33**, 171 (1994)

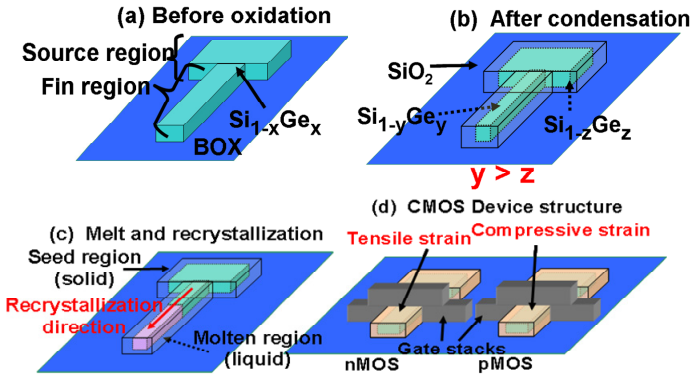


Fig. 1 The conceptual images of the proposed fabrication

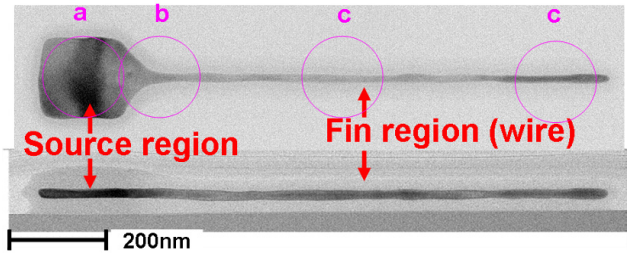


Fig. 3 The top-view and cross-sectional TEM images of the sample after recrystallization.

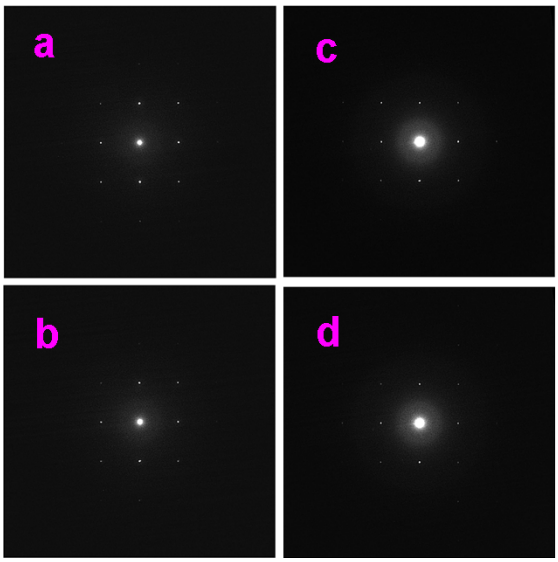


Fig. 5 Electron-beam diffraction patterns of the sample after recrystallization. Letters represent points in Fig. 3.

Table. 1
The strain in the Fin region, which was estimated from Tsang's formula [8]. The Ge concentration is determined by EDX analysis.

	Before melt	After recrystallization
Ge concentration estimated by EDX (%)	91	79
strain (%)	3.6	−0.2

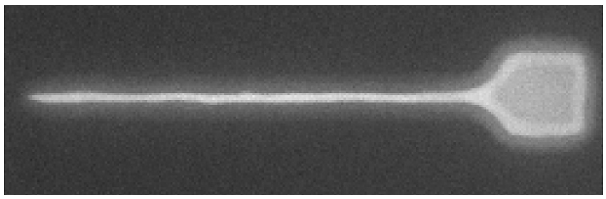


Fig. 2 HAADF-STEM image of the sample after Ge condensation process. The darker contrast represents lower Ge fraction.

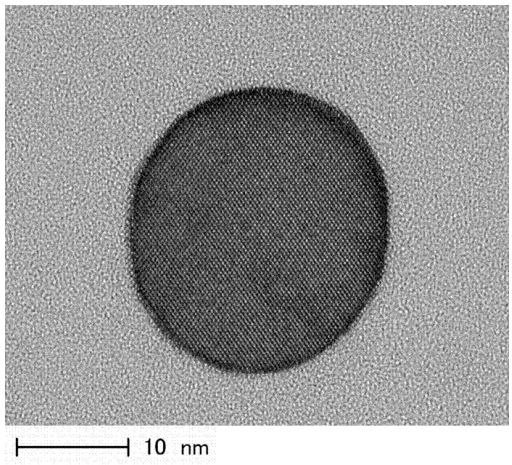
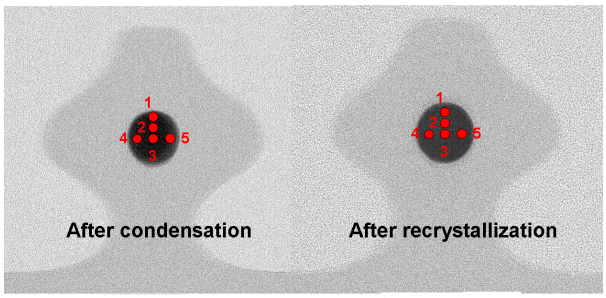


Fig. 4 The high-resolution cross-sectional TEM image of the sample after recrystallization.



	Ge concentration (%)	
point1	90.3	78.2
point2	92.6	78.5
point3	93.0	80.4
point4	89.5	77.8
point5	90.4	78.5

Fig. 6 Cross-sectional TEM image and EDX analysis.

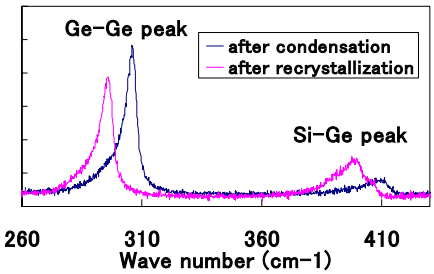


Fig. 7 Raman spectra of the Fin region before and after the recrystallization.