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Fabrication of Poly-Si TFT on Polycarbonate Substrate at Temperatures below 135°C

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1. Introduction

Thin film transistors (TFTs) create new values of large-area electronics not only by facilitating the performance of silicon-based TFTs but also by introducing new materials such as polymers and ceramic. TFTs on polymer substrate are being extensively studied since they have potential application to the flexible flat panel display that requires lighter weight, thinner film, flexibility and robustness. If TFTs whose carrier mobility is of a few tens cm^2/Vs are provided, high electronic functions can be integrated on the flexible substrate. Polycrystalline Si (poly-Si) is a promising material to realize such TFTs. Recently, operation of low temperature poly-Si TFT fabricated on the polyethersulphone (PES) substrate have been reported[1] to demonstrate the potential application of laser annealing.

When a polymer is used as the substrate material for low temperature poly-Si TFT, the processing of TFTs including poly-Si film formation, source/drain (S/D) activation, and gate insulator formation must be carried out at temperatures lower than the glass transition temperature (T_g) of the polymer. T_g is important parameter as well as coefficient of thermal expansion (CTE) to prevent the curling or vending of the substrate heated at not only crystallization step but also S/D activation step. The use of the polymer which has high T_g is one of the effective method to solve this problem. However, high T_g polymers such as polyimide (PI) are commonly expensive for the application to large-area consumer electronics. PI has also the drawback of opaque.

On the contrary to PI, polycarbonate (PC) is optically clear for visible light, possesses good mechanical property, and is much cheaper than PI. Therefore, if poly-Si TFTs are able to be fabricated on PC, the progress of large-area flexible electronics will be greatly facilitated. In this report, we demonstrate the fabrication of poly-Si TFTs on PC substrate at temperatures below 135°C, i.e. well below T_g of PC. The results indicate that TFTs whose electron mobility is over 10 cm^2/Vs can be fabricated.

2. TFT fabrication

Figure 1 shows schematic cross-section of poly-Si TFT fabricated on PC substrate. T_g, CTE and thermal shrinkage at 180°C of PC substrate (TEIJIN SS120) which were used in our study are 215°C, 70 ppm and <0.01%, respectively. Amorphous Si (a-Si) film with a thickness of 180 nm on the buffer-SiO_2 film with a thickness of 220 nm was deposited on the SS120 substrate by RF magnetron sputtering. Frequency, RF power, substrate temperature and background pressure of RF magnetron sputtering are 13.56 MHz, 50 W, room temperature and below 10^{-5} Pa, respectively. Third harmonics of an Nd:YAG laser (λ=355 nm, 100 shots, 0.3 W) were irradiated at an energy density ranging from 200 to 233 mJ/cm^2 in the air and at room temperature to crystallize the a-Si precursor film. Pulse duration of the laser was 5 ns at full width at half maximum.

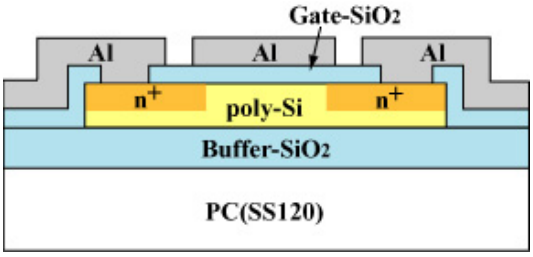

Fig. 1: Schematic cross-section of n-channel top-gate poly-Si TFT on PC substrate.

Figure 2 shows a scanning electron microscope (SEM) image of poly-Si film on the SS120 after the laser irradiation at 233 mJ/cm^2. Prior to SEM observation, Si crystal grains were delineated by Secco's etching. No damaged poly-Si film was observed under the present experimental condition. One of the reasons of this is owing to the low thermal shrinkage of SS120[2]. Poly-Si grains with diameter from 70 to 90 nm were observed.

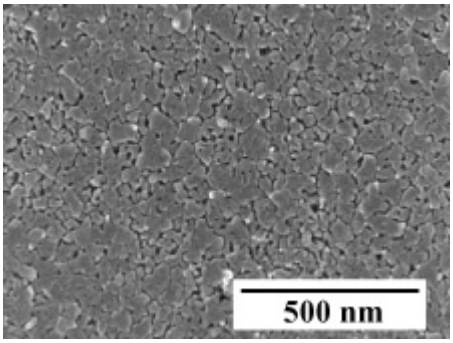

Fig. 2: SEM image of poly-Si film on SS120 after the laser irradiation at 233 mJ/cm^2. The poly-Si film surface was delineated by Secco's etching.

After patterning the active region of TFTs by photolithography and reactive ion etching (RIE) with CF_4 plasma, S/D was formed by ion implantation of phosphorous (35 keV, $3x10^{15}$ cm^{-2}). Dopant activation was done by Nd:YAG laser

irradiation at 200 mJ/cm^2. Figure 3 shows laser shot number dependence of sheet resistance at n$^+$-activated poly-Si film. The sheet resistance decreases with increasing shot numbers independent of the wave length. However, the sheet resistance and its dispersion of Si film activated by using second harmonics of an Nd:YAG laser (λ=532 nm) is lower than that activated by using third harmonics of an Nd:YAG laser (λ=355 nm). The results indicate that the whole doped region in terms of in-depth direction is effectively annealed since the penetration depth of second harmonics of an Nd:YAG laser is larger than that of third harmonics of an Nd:YAG laser. The resistivity in the case where the doped region was activated by 500 shots irradiation of second harmonics was estimated to be 4.7 mΩcm by assuming a uniform in-depth carrier profile.

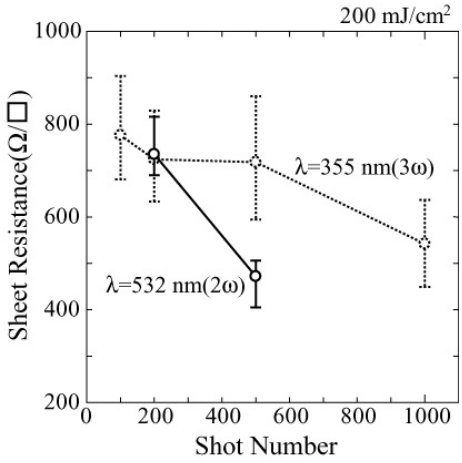

Fig. 3: Sheet resistance at n$^+$-activated poly-Si film as a function of laser shot number.

The gate SiO_2 film with a thickness of 100 nm was deposited by RF magnetron sputtering under the condition of RF power = 100 W, substrate temperature = room temperature, background pressure = 3x10^{-5} Pa. Then the contact holes were opened by photolithography and wet etching. Finally, Al gate electrode was formed by using a lift-off process. The maximum substrate temperature in our process is 135°C required for the baking of the resist during photolithography. Figure 4 shows an optical micrograph of a poly-Si TFT fabricated on the SS120 at temperatures below 135°C.

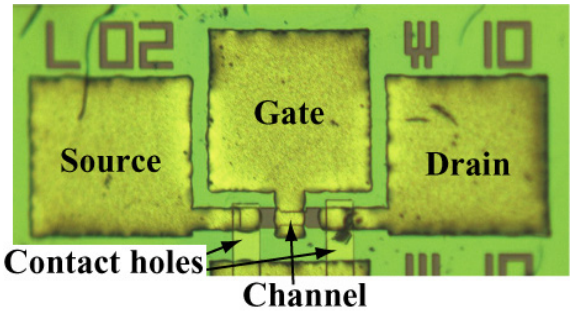

Fig. 4: Optical micrograph of poly-Si TFT fabricated on SS120 at temperatures below 135°C.

3. Performance of poly-Si TFT on PC(SS120)

We measured the characteristics of the n-channel top-gate poly-Si TFT on the SS120. The gate length/gate width (L/W) is 2/5 μm. Figure 5(a) shows transfer characteristic of poly-Si TFT on the SS120 measured at the source-to-drain voltage (V_{DS}) of 2 V. The on/off ratio of TFT is approximately 10^2. This results from the leakage current at the drain contact. It is considered that the drain leakage current can be reduced by thinning poly-Si active layer. Figure 5(b) shows output characteristics of poly-Si TFT on the SS120 measured at the gate voltages (V_{GS}) from 1 to 6 V. The operation of TFT is clearly obtained. The maximum carrier mobility of poly-Si TFT on the SS120 was 22.5 cm^2/Vs, and average carrier mobility of these devices was 3.3 cm^2/Vs. These values are from 30 to 200 times larger than the carrier mobility of conventional a-Si TFTs.

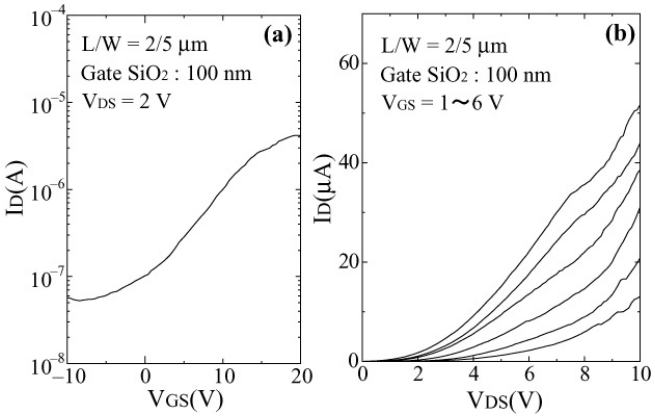

Fig. 5: (a) Transfer characteristic and (b) output characteristics of poly-Si TFT on SS120.

4. Conclusions

Poly-Si films having grain size of about 100 nm can be prepared without any damage on PC substrate by using irradiation of λ=355 nm laser pulses generated by Nd:YAG laser. Low resistance S/D can be formed by combining ion implantation and λ=532 nm laser irradiation. TFTs fabricated at temperatures below 135°C by employing sputter deposited gate SiO_2 shows carrier mobility over 10 cm^2/Vs while suppression of leakage current remains as an issue. We conclude that low temperature poly-Si TFT is a promising device for large-area flexible electronics.

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