Strain-Induced Back Channel Electron Mobility Enhancement in Poly-Si TFTs Formed by Continuous-Wave Laser Lateral Crystallization

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1. Introduction
High performance poly-Si TFTs with high carrier mobility are expected for a system on glass application. To enhance the mobility, various laser crystallization processes to enlarge grain size have been developed [1-5]. Among them, continuous-wave (CW) laser lateral crystallization (CLC) can form the longest grains [3-5]. It has been found that CLC poly-Si films have tensile strain [4, 5]. However, the strain effect to the mobility has not been clarified yet although strain modulates mobility [6]. In this study, 4-terminal (4T) CLC poly-Si TFTs having both front and back gates were fabricated and the strain effect was investigated by comparing front channel mobility (μeff, front) with back channel mobility (μeff, back).

2. Experiments
Figure 1 shows the process flow. In CLC (λ=532 nm), the laser spot size was 90×20 μm² (FWHM) with a Gaussian profile. Figure 2 shows cross-sectional schematic images of the CLC poly-Si TFTs. For comparison, 3-terminal (3T) CLC poly-Si TFTs (front channel operation, not having back gates) were also fabricated. The channel direction was parallel to the laser scanning direction. Both the gate length (L) and gate width (W) were 10 μm. Both the front and back interfaces were estimated at ~0.3% (FWHM) with a (111) peak 20 dependence on the incident angle in X-ray diffraction (XRD) measurement in the in-plane direction. As the incident angle increased, the peak 20 decreased. This result shows that the back interface had larger tensile strain than the surface. The strain values at the surface and back interfaces were estimated at ~0.3% and 0.4% or larger, respectively. Figures 7(a) and 7(b) show the ID-VGS characteristics of 4T CLC poly-Si TFTs in front and back channel operation, respectively. Vth (VGS at ID=1×10⁻⁷ A) was controlled by VBACK or VFRONT. Figure 8 shows Vth dependence on VBACK or VFRONT. The slopes in Fig. 8 showed the body factor (γ). In both front and back channel operation, γSTANDBY and γACTIVE were 0.8 and 1.2 V/V, respectively. In the case of TFOX=TBOX=TOX, Vth dependence on (3TOX)/3TOX, respectively [8]. In this study, theoretical values of γSTANDBY and γACTIVE were 0.80 and 1.25 V/V, respectively. Successful operation of variable Vth scheme in both front and back channel operation was achieved. To comparing μeff, front with μeff, back, 4T CLC poly-Si TFTs were biased into a standby state so as not to form the inversion layer on the Vth-control gate side. Figure 9 shows typical characteristics of μeff, front and μeff, back dependences on NINV. μeff, back was larger than μeff, front. Figure 10 shows the relationship between μeff, front and μeff, back. The enhancement factor (μeff, back/μeff, front) was 1.2, which was comparable with that in strained SOI MOSFETs [9]. It was found that the larger tensile strain around back interface enhanced μeff, back.

4. Conclusions
4T CLC poly-Si TFTs were fabricated to investigate the effect of tensile strain induced by CLC. The strain values at the surface and back interfaces were estimated at ~0.3% and 0.4% or larger, respectively. Because of the larger tensile strain, μeff, back was 1.2 times larger than μeff, front. Back channel operation in CLC poly-Si TFTs is useful for enhancing the CLC poly-Si TFT performance.

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References
Processes for 4T CLC poly-Si TFTs:
- a-Si deposition (LPCVD, 150 nm) on quartz substrates
- B" implantation for back gate (30 keV, 2 × 10^{15} cm^{-2})
- Activation (N\textsubscript{2}, 900°C, 1 h)
- SiO\textsubscript{2} deposition (APCVD, 200 nm)
- Anneal (O\textsubscript{2}, 900°C, 1 h)
- a-Si deposition (LPCVD, 150 nm)
- Cap SiO\textsubscript{2} deposition (APCVD, 25 nm)
- CLC (4.7 W, 20 cm/s)

Fig. 1 Process flow.

Cap SiO\textsubscript{2} etching
As\textsuperscript{+} implantation for S/D region (25 keV, 2 × 10^{15} cm^{-2})
Activation (N\textsubscript{2}, 900°C, 2 h)
Active etching
SiO\textsubscript{2} deposition (APCVD, 200 nm)
Anneal (O\textsubscript{2}, 900°C, 1 h)
Contact etching
Al evaporation & patterning
Sintering (N\textsubscript{2}/H\textsubscript{2}, 400°C, 30 min)

Processes for 3T CLC poly-Si TFTs:
- a-Si deposition (LPCVD, 150 nm)
- B" implantation for back gate (30 keV, 2 × 10^{15} cm^{-2})
- Activation (N\textsubscript{2}, 900°C, 1 h)
- SiO\textsubscript{2} deposition (APCVD, 200 nm)
- Anneal (O\textsubscript{2}, 900°C, 1 h)
- a-Si deposition (LPCVD, 150 nm)
- Cap SiO\textsubscript{2} deposition (APCVD, 25 nm)
- CLC (4.7 W, 20 cm/s)

Fig. 1 Process flow.

Fig. 2 Cross-sectional schematic images. (a) 4T CLC poly-Si TFT. (b) 3T CLC poly-Si TFT.

Fig. 3 EBSD mappings of the channel poly-Si films. (a) 4T CLC poly-Si TFT. (b) 3T CLC poly-Si TFT.

Fig. 4 Average \(\mu_{\text{eff, front}}\) and its standard deviation.

Fig. 5 Typical characteristics of \(\mu_{\text{eff, front}}\) dependence on \(N_{\text{inv}}\).

Fig. 6 (111) peak 20 dependence on the incident angle in XRD measurement in in-plane direction.

Fig. 7 \(I_{\text{DS}}-V_{\text{GS}}\) characteristics of 4T CLC poly-Si TFT. (a) Front channel operation. (b) Back channel operation.

Fig. 8 \(V_{\text{th}}\) dependence on \(V_{\text{BACK}}\) or \(V_{\text{FRONT}}\).

Fig. 9 Typical characteristics of \(\mu_{\text{eff, back}}\) and \(\mu_{\text{eff, front}}\) dependences on \(N_{\text{inv}}\).

Fig. 10 Relationship between \(\mu_{\text{eff, front}}\) and \(\mu_{\text{eff, back}}\).