Fabrication of Ge-MOS Capacitors with High-Quality Interface by Ultra-Thin SiO2/GeO2 Bi-Layer Passivation

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1. Introduction

Ge is of great interest as a candidate channel material for future CMOS devices due to its higher intrinsic carrier mobility. To realize Ge-CMOS technology, one of the most challenging issues is formation of a good MOS stack. The attractive interface passivation methods are to grow Ge compounds such as GeO2, Ge3N4, and GeO2N2. In particular, GeO2/Ge structure has superior interface property. Matsubara et al. have reported the low interface state density (DIt) of 1×1011 cm-2eV-1 [1], which was formed by dry oxidation at around 575 °C.

However, GeO2 is difficult to integrate into MOS fabrication process due to its poor thermal stability and water solubility. It has been pointed out that not only water but also hydrocarbons are easily infiltrated into GeO2 layers during air exposure, causing to unusual negative shift of flat band voltage (Vfb) and large increase in hysteresis (HT) in capacitance-voltage (C-V) curve [2].

If very thin SiO2/GeO2 bi-layer can be formed on Ge substrate without air exposure, such bi-layer should be very useful as interlayer (IL) between gate insulating film and Ge substrate, because GeO2 and SiO2 layers act as passivation films of Ge surface and GeO2 layer, respectively. Furthermore, if high-k film such as HfO2 or ZrO2 is deposited on Ge substrate with bi-layer passivation (BLP), it is expected that high-k film with low EOT (effective oxide thickness) and low DIt should be realized on Ge substrate.

In this study, we propose a novel method for electrical passivation of Ge surface by ultra-thin SiO2/GeO2 bi-layer, which is processed in the physical vapor deposition (PVD) system through the thermal etching of GeO2 by vacuum annealing at around 550 °C and the subsequent SiO2 deposition with low rate at 350 °C. We demonstrate the validity of BLP from DIt measurements for MOS capacitors.

2. Experimental

We investigated the preparation condition for BLP using PVD (RF magnetron sputtering), which enables us to anneal under high vacuum condition. Schematic process flow is shown in Fig. 1. Here, p-type (100) Ge substrates with a resistivity of 0.2-0.3 Ωcm were used. After wet chemical cleaning, the sacrificial oxidation was done at 450°C for 30 min in O2, by which GeO2 layer thickness was 3.2 nm. The sample was loaded in PVD chamber, which was subsequently pumped down to base pressure of less than 2×10-5 Pa and immediately heated to a temperature (T30) of 350 °C for SiO2 deposition by lamp heater. Here, it is noted that we selected the step mode heating so that the sample temperature increased up to around 550 °C and decreased down to T30 of 350 °C during 5 min, which led to volatilization of GeO2 layer.

1 nm-thick SiO2-interlayer (IL) deposition on the cleaned Ge surface, after being maintained at T30 for 30 min, was performed without breaking vacuum. The details for IL deposition are as follows: The SiO2 target was used for the IL-deposition. We selected two modes with and without O2 addition in Ar gas during sputtering; For the case of O2 addition, the gas pressure was kept at 1.0 Pa with Ar and O2 flow rates of 20 and 0.2 sccm, respectively, and the rf power was 13 W, resulting in the deposition rate of 0.11 nm/min; For the case of no O2 addition, the gas pressure was also kept at 1.0 Pa with an Ar flow rate of 20 sccm and the rf power was 10 W, resulting in the deposition rate of 0.11 nm/min.

In order to clarify the structures after SiO2-IL deposition, XPS measurements using an Al Kα line were carried out for the samples with and without O2 addition. Figure 2(a) shows the Ge 3d XPS spectra. The SiO2 signals with binding energy (BE) of 103.4 eV were clearly observed for both samples. For the sample without O2, oxidized Ge 3d peaks could not be observed. This implies that initial GeO2 layer was completely removed by vacuum annealing and the subsequent GeO2 formation did not occur.

Fig. 1. Schematic diagram of the process flow for sample preparation.

Fig. 2. XPS spectra for (a) SiO2-IL/Ge samples deposited with and without O2, and (b) thermally grown GeO2/Ge samples.
On the other hand, the sample with O₂ showed clear oxidized Ge 3d peak, which shifts to higher BE by 3.3 eV relative to the Ge bulk peak (29.3 eV) [3], implying that the signal with BE of 32.6 eV is mostly originated from GeO₂. In Fig. 2 (b), the spectra of thermally grown GeO₂/Ge samples with thicknesses of 1.0, 1.5, and 2.4 nm, which were prepared at 400 °C for 9 min, 400 °C for 22 min, 450°C for 18 min, respectively, were used as reference for thickness of GeO₂ underlying SiO₂-IL. The signal intensity ratio of GeO₂ to Ge bulk for the sample with O₂ is close to that for 1.5 nm-thick GeO₂/Ge sample. Thus, the thickness of GeO₂ just after BLP is around 1.0 nm. Since the EOT of GeO₂ for 400°C-PDA sample was 0.7 nm, the corresponding physical thickness was 1.0 nm. Thus, we infer that the thickness of GeO₂ underlying SiO₂-IL should be less than 1.5 nm, because 1 nm-SiO₂-IL causes to decrease the intensity of Ge bulk XPS signal, which is confirmed from electrical measurement of MOS capacitor, as mentioned later.

We fabricated SiO₂-ILs using four kinds of preparation methods. They are labeled to as samples #1-4; The sample #1 was prepared through the process flow of (a) → (b) → (c) → (d) in Fig. 1; #2 was (a) → (b) → (c) → (e); #3 was (a) → (c) → (d); #4 was only (a). After such preparations, the 10 nm-thick SiO₂ film with O₂ addition was deposited on each sample at room temperature (RT) using the same PVD system and followed by post-deposition annealing (PDA) at 550 °C for 30 min, which was the same for all samples. Here, the SiO₂ film deposition was performed under the gas pressure of 1.0 Pa with Ar and O₂ flow rates of 20 and 0.2 sccm, respectively. The capacitor #5 was fabricated by 10 nm-SiO₂ deposition without O₂ addition after the same IL formation as capacitor #1. Finally, Al gate electrodes with area of 4.5×10⁻⁴ cm² were patterned by lithography and wet etching.

3. Results and discussion

Figure 3 (a) shows C-V(G) curve of MOS capacitor labeled to as #1, where the measurement was performed at RT and at a frequency (f) of 1 MHz. The bias was double-scanned from +1 to -1 V. The EOT, HT, and Vfb were obtained as 12.5 nm, 0.22 V, and -0.73 V, respectively. The fixed charge density was estimated as +5.5×10¹¹ cm⁻² from the value of Vfb using the work function (4.1 eV) of Al on SiO₂, which was almost the same order as that of SiO₂/Si. By using the values of the EOT and the deposited SiO₂ thicknesses, the EOT of GeO₂ layer underlying SiO₂-IL was estimated as 1.1 nm. Furthermore, the EOT for the sample with 400 °C-PDA was lower by 0.4 nm relative to 550 °C-PDA sample. This means that re-growth of GeO₂ layer occurred during 550 °C-PDA. The physical thickness of re-growth GeO₂ was estimated as 0.6 nm taking into account that k-value of GeO₂ is 5.7. Since the EOT of GeO₂ for 400°C-PDA sample was 0.7 nm, the corresponding physical thickness was 1.0 nm. Thus, we infer that the thickness of GeO₂ just after BLP is around 1.0 nm.

It was also found from Fig. 2 (b) that J–E curve of capacitor #1 shows excellent insulating feature governed by Fowler-Nordheim tunneling and high breakdown field (Eb) of 14 MV/cm. Other MOS capacitors (#2-4) also showed the similar properties to that of #1, implying that parameters such as HT, Vfb, and Eb of MOS capacitors were governed by the deposition of SiO₂ insulating film and the subsequent PDA.

However, Dₖ was strongly dependent on IL preparation. Figure 4 shows Dₖ results for MOS capacitors labeled to as #1-5. The evaluations were done by DLTS. The Dₖ values at around midgap are indicated in Fig. 4. The best Dₖ of 3.7×10¹¹ cm⁻²eV⁻¹ was obtained for the capacitor #5, which is approximately 3 times lower than that of capacitor #4. Thus, we can conclude from the Dₖ results that 1. sacrificial oxidation and the subsequent surface cleaning in vacuum are useful for the decrease in Dₖ; 2. the BLP with structure of SiO₂/GeO₂/Ge is much better than that with SiO₂/Ge; 3. the deposition of oxygen-rich SiO₂ insulating film is harmful to interface quality, implying that excessive oxygen may degrade quality of the GeO₂ passivation layer. Therefore, a proper control of total oxygen content is important for interface quality optimization.

4. Conclusion

We established an effective electrical passivation method of Ge surface by ultra-thin SiO₂/GeO₂ bi-layer, which can be processed in the PVD system through the thermal etching of GeO₂ by vacuum annealing at 550 °C and the subsequent SiO₂ deposition at 350°C. We demonstrated the validity of this passivation technique from Dₖ measurements for MOS capacitors. The Dₖ of 3.7×10¹¹ cm⁻²eV⁻¹ at around midgap was achieved under optimum condition, which is 3 times lower than that of no-passivated capacitor.

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References