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Improvement of The Property of FET Having The HfO_2/Ge Structure Fabricated by Photo-Assisted MOCVD with Fluorine Treatment

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1. Introduction

As the scaling of advanced integrated circuits is approaching its technological and physical limits, new materials for metal-oxide-semiconductor field effect transistor (MOSFET) are needed to further improve the performances. Therefore, hafnium oxide (HfO_2) has attracted much attention for application as a gate insulator film recently. Moreover, germanium (Ge) is highlighted as a candidate semiconductor for high speed transistor, as it has higher electron and hole mobility than those of Si [1]. However, the dielectrics deposited on Ge surface last-treated by diluted HF exhibit large interface state, since Ge surface is not passivated easily by hydrogen (H) [2]. To solve this problem, it is necessary to passivate the Ge surface by a proper element before dielectric layer deposition. To achieve that, the passivation of the Ge surface using new treatment materials (AlN_x, Ba, S, La) is studied to reduce interface state [3-6]. We also reported that fluorine (F) treatment is more effective than hydrogen on Ge substrate [7].

In this paper, the HfO_2/Ge MISFET device has been prepared by using a new F-treatment mechanism on Ge surface to reduce interface state of HfO_2/Ge gate stack. As a result, we were able to improve the electric properties of HfO_2/Ge MISFET device.

2. Experimental Details

N-type Ge(100) wafers with a resistivity of 1~10 Ωcm were first cleaned in a 10% HF solution for 10 min, to remove the native GeO_x layer. After wet cleaning treatment, HfO_2 thin films were prepared on the Ge wafers by using photo-assisted MOCVD [8]. Photo-assisted MOCVD can improve the film quality to enhance the reaction with source materials by ultraviolet irradiation. Next, to reduce interface states of HfO_2/Ge gate stack, we fabricated HfO_2 insulation films on the Ge wafer by three processes (Fig 1-(A)). The 1st sample consisted of only 25 layers (1 layer is about 2 nm) HfO_2 thin film by using $Hf(O\text{-}t\text{-}C_4H_9)_4$ and H_2O combination at 300˚C (not-treated sample). The 2nd sample was treated in F_2 gas (F_2/He = 5 %/95 %) ambient to make F-Ge bonding at Ge surface prior to HfO_2 deposition (F-pretreatment sample ; FPT sample) [7]. The treatments were carried out at 0.2 Torr for 3 min, and treatment temperature was 50˚C. Finally, the 3rd sample was treated by F_2 gas for 10 sec before each HfO_2 deposition on the three bottom layers (FT3 sample). After making the insulation layer, all samples were annealed at 300˚C for 30 min in N_2 ambient (PDA). Next, Pt (top) and

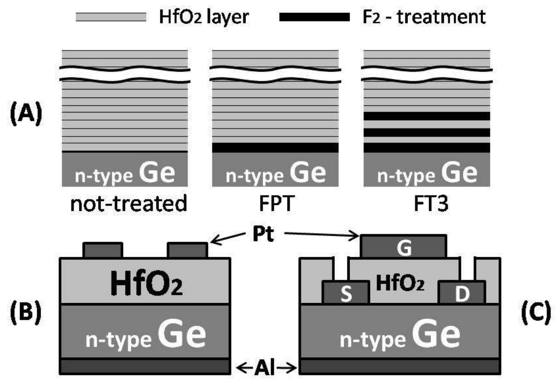

Fig. 1 Three types of HfO_2 thin films on Ge wafer prepared without or with F_2-treatment (A), schematic illustration of HfO_2/Ge MIS (B) and MISFET (C) devices.

Al (bottom) electrodes were formed by sputtering and thermal deposition. Finally, PMA was performed at 300˚C for 30 min in N_2 ambient. Fig 1-(B) shows the structure of the MIS device fabricated by this process. Next, we made HfO_2/Ge MISFET devices by photolithographic approach (Fig 1-(C)). HfO_2 thin films were deposited using the same three ways (not treated, FPT and FT3) on MIS process.

The incorporated F amounts in HfO_2/Ge gate stack were characterized by XPS and TDS. There are also other measuring methods such as Terman method, current method and conductance method. Finally, we calculated mobility of the HfO_2/Ge FET device after I_s-V_d property measurement.

3. Results and discussion

Figure 2 shows the F 1s photoelectron spectra on the Ge surface after F_2-treatment by the three above-mentioned processes. As shown in this figure, F was adsorbed on Ge

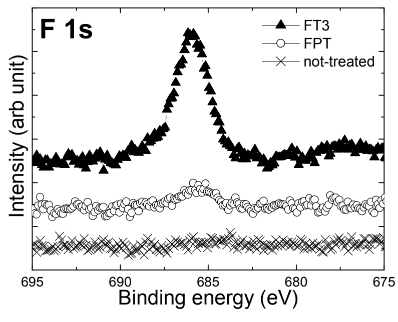

Fig. 2 F 1s photoelectron spectra Ge surface after F_2-treatment by XPS.

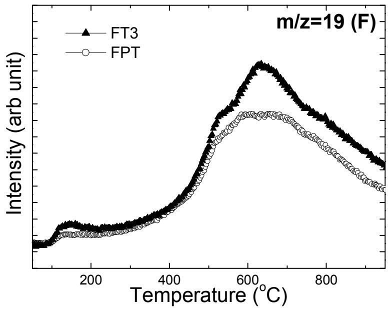

Fig. 3 Thermal desorption spectra of F (m/z=19) from HfO_2/Ge gate stack prepared by various F_2-treatment

surface by F_2-treatment. Although the FPT sample does not show distinct difference of F 1s peaks with the not-treated sample without treatment, a large peak of F 1s was observed on the FT3 sample. As a conclusion, we can confirm that more F remains on the FT3 sample than on any of the other samples. This suggested that F was more easily incorporated with HfO_2 on Ge surface than without Hf.

The thermal desorption spectra of F from HfO_2/Ge gate stacks are presented in Figure 3. We can observe that a lot of the F were out-diffused from FPT and FT3 samples at high temperature. Especially, in the vicinity of 600°C, the desorbed F amounts on FT3 sample increase more than on the FPT sample. It is thought that F is densely-distributed at the interface between the HfO_2 thin film and the Ge wafer by FT3-treatment system. According to the results of XPS and TDS, it is expected that interface traps on the FT3 sample are more passivated than other samples.

Figure 4 shows energy distribution of the interface state densities (D_{it}) for not-treated, FPT and FT3 samples measured by DLTS. Among the three samples, the FT3 sample has the lowest D_{it} on both mid-gap and shallow gap states. It is believed that the amount of poorly passivated dangling bond and oxygen vacancy near the interface between HfO_2 and Ge surface could be decreased by superior F. This suggests that the F_2-treatment with HfO_2 on Ge surface (FT3 sample) prior to HfO_2 deposition is very effective for improving the properties of HfO_2/Ge interface.

Finally, figure 5 shows the variation of the source current on HfO_2/Ge MISFET device by applied drain and gate voltage. As shown in the figure, we can say that the current value is increased by the F_2-treatment. Moreover, the calculated peak mobility of FET using not-treated, FPT and FT3 samples are about 322, 405 and 442 cm^2/Vs respectively.

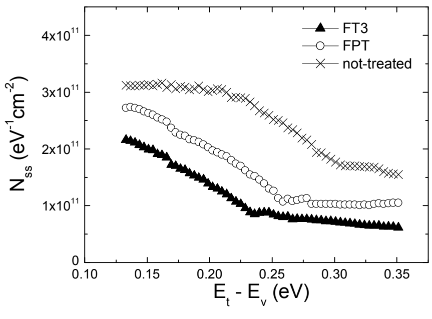

Fig. 4 Energy distribution of interface state densities (D_{it}) for various F_2-treatment measured by DLTS

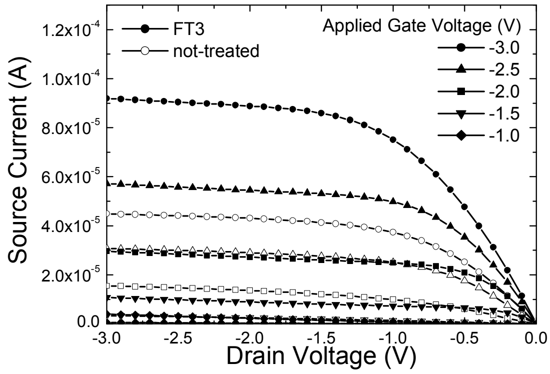

Fig. 5 I_s – V_d characteristics of HfO_2/Ge MISFET device with and without F_2 – treatment.

We were able to observe that the C-V characteristic of HfO_2/Ge gate stack is improved by F_2-treatment, too. However, large hysteresis remained on the gate stack. It is thought that the traps other than the poorly passivated Ge dangling bond are not removed perfectly from the HfO_2 thin film. As a result of trying to solve the problem, we succeeded in fabricating HfO_2/Ge MIS device which has good C-V characteristic by low depo-temperature condition. We also believe that Ge-based MISFET device which has higher mobility can be obtained, in the near future.

4. Conclusions

In this study, we have fabricated a HfO_2/Ge MISFET device using a new F_2-treatment mechanism. We establish that after performing the F_2-treatment with HfO_2 deposition, a lot of F exists in the interface of HfO_2/Ge gate stack. Consequently, interface traps in the gate stack were passivated by F and interface state densities (D_{it}) were decreased. Therefore, we were able to fabricate a high speed HfO_2/Ge MISFET device.

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