# Electrical characterization of wafer-bonded germanium-on-insulator substrates using a four-point-probe pseudo-MOSFET

Yuji Iwasaki<sup>1</sup>, Yoshiaki Nakamura<sup>1</sup>, Jun Kikkawa<sup>1</sup>, Akira Sakai<sup>1</sup>, Motoki Sato<sup>2</sup>, Eiji Toyoda<sup>2</sup>, Hiromichi Isogai<sup>2</sup>, Koji Izunome<sup>2</sup>

<sup>1</sup>Osaka University, 1-3 Machikaneyama, Toyonaka, Osaka 560-8531, Japan Phone: 81-6-6850-6301, E-mail: nakamura@ee.es.osaka-u.ac.jp, Phone: 81-6-6850-6300, E-mail: sakai@ee.es.osaka-u.ac.jp <sup>2</sup>Covalent Silicon Co., Ltd., 6-861-5 Higashikou, Seirou-machi, Kitakanbara-gun, Niigata 957-0197, Japan

### 1. Introduction

Using germanium-on-insulator (GOI) substrates as a transistor channel is promising for producing next-generation transistors because of its high carrier mobilities. In the methods for fabricating GOI substrates, wafer bonding technique [1] offers higher quality Ge layers and buried oxide layer in GOI substrates. However, the fabrication process of GOI substrates based on the wafer-bonding technique has not been optimized yet. To achieve this it is essential to systematically evaluate the electrical characteristics of GOI substrates.

The pseudo-MOSFET technique is one of the simplest methods for determining the electrical characteristics. One advantage in this technique is convenience that results from using two metal probes rather than source and drain electrodes. However, the accuracy of this technique is relatively low due to the contact resistance, the complexity of the electrical field between the two probes, and the difficulty in determining the geometrical factor  $f_g$ , which is required to determine the carrier mobility. The four-point-probe pseudo-MOSFET technique is very promising because it eliminates any contact resistant due to their four-terminal method and is performed using four regularly aligned probe electrodes whose  $f_g$  value is well known.

In this study, we use a four-point probe pseudo-MOSFET to measure the electrical characteristics of wafer-bonded GOI substrates annealed at various temperatures in vacuum. We confirm transistor operation of the annealed GOI substrates and measure their carrier mobilities in channel layer,  $\mu_0$  and the interface trap densities,  $D_{it}$ . The dependence of the electrical characteristics on the annealing temperature can be explained in terms of the influence of the defect states on energy band bending.

## 2. Experimental

GOI substrates were fabricated by wafer bonding of Ge(001) substrates and Si(001) substrates that have SiO<sub>2</sub> films as follows. 400-nm-thick SiO<sub>2</sub> films were formed on p-type Si(001) substrates doped with boron  $(3 \times 10^{15} \text{ cm}^{-3})$  by dry oxidation at 1200°C for 1 h. The Si substrates with SiO<sub>2</sub> films and non-doped Ge(001) substrates were bonded and then were annealed for 1 h at 300°C in a N<sub>2</sub> atmosphere

(2 Pa). The Ge layers of the bonded wafers were mechanically thinned to 200 nm to form GOI substrates. The GOI substrates were annealed at  $T (= 400-600^{\circ}\text{C})$  for 1 h in vacuum at a pressure of  $10^{-3}$  Pa to strengthen the bonding.

To perform the pseudo-MOSFET measurement, circular Ge mesa structures with diameters of 4 mm are fabricated by photolithography and etching to prevent current leakage through the side surfaces of the wafer. The electrical measurements were performed by contacting the four probes with the Ge mesa surfaces. The four probes were made of tungsten carbide and were arranged linearly with a pitch of 0.1 mm. In this system,  $f_g$ , is considered to be 4.54 [2]. Gate voltage,  $V_G$  was applied to the back side of the Si substrate through the Al back gate electrode with a reference to electric potential of the Ge mesa surface. We performed two types of measurements. One uses the four-terminal method to remove the contact resistance. In this method, the voltage between the central two probes (the drain voltage  $V_D$ ) was measured as a function of  $V_{\rm G}$  while keeping the current between the two probes at the both ends of aligned 4 probes (the drain current  $I_D$ ) to be constant at 500 nA. From this measurement, we obtained the channel conductance  $G=dI_D/dV_D$  as a function of  $V_G$ . The other measurement is a simple two-terminal measurement that is to obtain  $I_D$ - $V_G$ curves using two neighboring probes  $(I_D)$ .

## 3. Results

Transistor operation of all the GOI was confirmed in channel conductance, G- $V_G$  curves as shown in Fig.1. The GOI annealed at lower than 500°C show n-channel depletion type behavior while for the GOI annealed at 550-600°C, the transistor operation was p-channel depletion type. The hysteresis loop in G- $V_G$  curves disappeared by annealing at higher temperature of 600°C.

To estimate the carrier mobility, we plotted the  $G/G^{0.5}$ - $V_{\rm G}$  curves with the following relation,

$$\frac{G}{\left(dG/dV_{G}\right)^{0.5}} = \frac{G}{G'^{0.5}} \sqrt{f_{g} \mu_{0} C_{OX}} \left(V_{G} - V_{T}\right) \quad , \quad (1)$$

where  $C_{\text{OX}}$  is the capacitance of the buried oxide and  $V_{\text{T}}$  is the threshold voltage. Using Eq. (1), we extracted the  $\mu_0$ 

from the slope of fitted lines as shown in Fig. 2. The carrier mobility estimated by this method were shown in Fig. 3. We found that the carrier mobility depended on the  $V_G$  sweep direction due to the hysteresis in the G- $V_G$  curves. Thus, the GOI samples annealed at 600°C, which did not exhibit hysteresis, have no dependence of the charier mobility on the  $V_G$  sweep direction. When the carrier mobilities extracted in the same  $V_G$  sweep direction were compared for GOI samples annealed at various temperatures, the carrier mobility was found to be highest for the sample annealed at 500°C.

The interface trap density,  $D_{it}$  was also estimated from  $I_D$ - $V_G$  curves obtained by the two-probe pseudo-MOSFET. The  $D_{it}$  was reduced with increase in the annealing temperature (not shown). This indicates that high temperature annealing process vanishes the interface defects.



Fig. 1  $\,$   $G\text{-}V_{\rm G}$  curves of GOI substrates annealed at (a) 500 and (b) 600°C



Fig. 2  $G/G^{.0.5}$ - $V_{\rm G}$  characteristics of GOI samples annealed at 500°C (this represents a typical curve).



Fig. 3 Dependence of channel carrier mobility on the annealing temperature. Two measurements were performed at two different places on the same GOI sample.

#### 4. Discussion

The hysteresis in G- $V_G$  curves indicated the presence of the interface defects, charged states of which are influenced

by the  $V_{\rm G}$  sweep directions. The variation of charged states can simultaneously change the carrier mobility through the Coulomb interaction. In this framework, it can be easily understood that the hysteresis and the dependence of carrier mobility on  $V_{\rm G}$  sweep direction both disappeared when the interface defects vanished by high temperature annealing.

Another remarkable finding is that the transistor operation of the GOI samples changes from n-channel depletion to p-channel depletion types with increasing annealing temperature. This differs greatly from the enhancement type characteristics of GOI substrates annealed in forming gas [3]. This type change is considered to be due to the change of energy band bending at the SiO<sub>2</sub>-Ge interface. In the case of a defect-free ideal junction of non-doped Ge substrates and SiO<sub>2</sub> on n-Si substrates. The energy band bends upward by 0.18 eV at the SiO<sub>2</sub>-Ge interface, as calculated from the difference in the work functions of p-type Si and non-doped Ge. In the samples annealed at low temperatures that exhibit n-channel depletion transistor operation, the energy band is expected to bend downwards in Ge layers near the SiO<sub>2</sub>-Ge interface. This downward bending indicates the presence of defect states with positive fixed charges at the interface, in the SiO<sub>2</sub> film, or in Ge layers near the interfaces. On the other hand, the samples annealed at high temperatures are expected to have an upward energy band bending. The change to upward bending is readily understood because high temperature annealing is expected to reduce the density of defect states, which cause the downward energy band bending. The change in the carrier type in the GOI samples can thus be explained by change in the energy band diagram due to the reduction in the defect state density by high temperature annealing.

#### 5. Conclusions

We used a four-point-probe pseudo-MOSFET to measure the electrical characteristics of wafer-bonded GOI substrates annealed in vacuum at various temperatures. We confirmed transistor operation of annealed GOI substrates and found that the channel type depended on the annealing temperature. The carrier mobility and the interface trap density were obtained from the electrical characteristics measured by the pseudo-MOSFET. The electrical characteristics strongly depend on the annealing temperature, which can be explained in terms of the influence of the defect states on energy band bending near the interface.

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