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High-Performance Poly-Si TFTs with Novel FinFet-like Channel

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Abstract

For the first time, we demonstrate a high performance TFTs with novel FinFet-like channel structure (FinFet-like channel TFTs, called FL-TFTs). The FL-TFTs exhibit low threshold voltage V_{TH}~0.5V, good subthreshold swing S.S.~ 240mV/dec. and high I_{ON}/I_{OFF} ratio>10^7 without any hydrogen-related plasma treatments. On the other hand, after Ni-salicidation and hydrogen-related plasma treatments, FL-TFTs exhibit steep subthreshold swing S.S.~ 190 mV/dec. and I_{ON}/I_{OFF} even higher than 10^8. The on-state currents can also be enhanced by Ni-salicidation.

Introduction

Multiple gate MOSFET architectures such as FinFETs are expected to be utilized beyond the 22nm node due to excellent SCE immunity[1]. From a transistor variation and mismatch perspective, FinFETs are considered particularly suitable for further SRAM scaling, thanks to their improved short channel effects behavior and lower channel doping concentration. Therefore, FinFET is the most promising double-gate transistor architecture [2] to extend scaling over planar device. On the other hand, high-performance low-temperature poly-Si thin film transistors (LTPS-TFTs) are recently developed for the employment of active-matrix liquid crystal displays on a glass substrate and for driving integrated circuits for the application of system-on-panel (SOP) and the three-dimensional (3-D) circuit integration elements such as SRAMs and DRAMs [3]–[5]. Besides, high-speed display driving circuits require thin film transistor (TFTs) to operate at low voltages and high driving currents, with a low threshold voltage. In this work, we demonstrate novel high performance TFTs with FinFETs-like channel by using very simple method. High-performance CFIN-TFTs of a low off leakage current, good S.S., and high I_{ON}/I_{OFF} ratio can be obtained, which are very promising for the realization of SOP and 3-D circuit integration.

Device Fabrication Process

Fig. 1 shows the process flow of the FL-TFTs in this work. First, the dummy layer with 150nm SiN and 150nm TEOS was deposited on the 500nm wet oxide [Fig. 1(a)]. After the dummy pattern was defined, a 50nm a-Si layer was deposited by low-pressure (LPCVD) [Fig. 1(b)]. Next, an annealing step was performed at 600℃ in N_2 ambient for 24 hrs to transform the a-Si into poly-Si, and dummy spacer was then formed [Fig. 1(b)]. Subsequently, source and drain region was defined, and the FinFet-like channel was formed by the reactive ion etching [Fig. 1(c)]. Then the TEOS dummy layer was removed [Fig. 1(d)]. 15nm chemical vapor deposition (CVD) oxide layer and 300-nm a-Si gate was deposited and patterned by reactive ion etching [Fig. 1(e)]. After the gate-stack formation, source and drain (S/D) regions were implanted with phosphorus, then activated with the TEOS spacer formation simultaneously. Ni-salicidation was achieved by RTA (rapid thermal annealing) at 450°C for 30sec. Finally, metallization and sintering were performed to complete the fabrication.

Results and Discussion

TRANSISTOR PERFORMANCE AND CHARACTERISTICS:

Fig.2 shows the scanning electron microscope (SEM) microphotograph of the FL-TFTs. The gate length of FL-TFTs is 0.35μm. Fig.3. shows the cross-section transmission electron microscope (TEM) micro-photograph of the FL-TFTs. Fig. 4 shows the I_D-V_G characteristics of FL-TFTs before any hydrogen- related plasma treatments and Ni-salicidation process. The FL-TFTs exhibit good swing~240 mV/dec and high I_{ON}/I_{OFF} ratio>10^7. In the Fig. 5, the FL-TFTs used the Ni-salicidation process and underwent the 30 min NH_3 plasma treatment, and the Control-TFTs with conventional planer process were also fabricated for comparison. The FL-TFTs shows the better I_D-V_G characteristics (SS~190 mV/dec. and I_{OFF}~10^{-14}, I_{ON}/I_{OFF} ratio~10^8) than the Control-TFTs (SS~450 mV/dec. and I_{OFF}~10^{-12}, I_{ON}/I_{OFF} ratio>10^6). The better performances of FL-TFTs can be attributed to the good gate control capability owing to the multiple gate structure. On the other hand, the FL-TFTs exhibit better performance after the Ni-salicidation process and the NH_3 plasma treatment. The on-state current can be significantly improved by reducing series resistance of S/D with Ni-salicidation and repairing the defect with the NH_3 plasma treatment. Fig. 6 shows the field-effect mobility μ_{FE} between the FL-TFTs and Control-TFTs. Furthermore, the FL-TFTs devices exhibit extremely high drive currents, as illustrated in Figs. 7. The high driving current would be very suitable for the application of SOP and 3-D circuit integration. TABLE I show device performance comparison between this work and published high performance TFTs data.

Conclusions

The high performance TFTs (FL-TFTs) with FinFet-like channel film has been proposed. The process is very simple and low cost. The FinFet-like structure can achieve a low off leakage current, good S.S., and high I_{ON}/I_{OFF} ratio simultaneously. The high performances of FL-TFTs can be attributed to the good gate control capability by the multiple gate structure. The high performances of FinFet-like structure would be very promising for the application of SOP.

References

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[3] Y. Oana et al., J. Soc. Inf. Disp., vol. 9, no. 3, pp. 169–172, 2001.
[4] F. Hayashi et al., IEDM Tech. Dig., pp. 283–286, 1996
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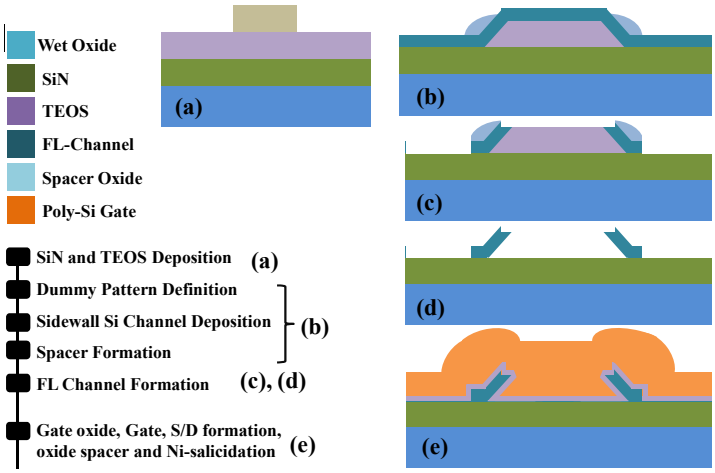

Fig. 1. Process flows of FL-TFTs in this work.

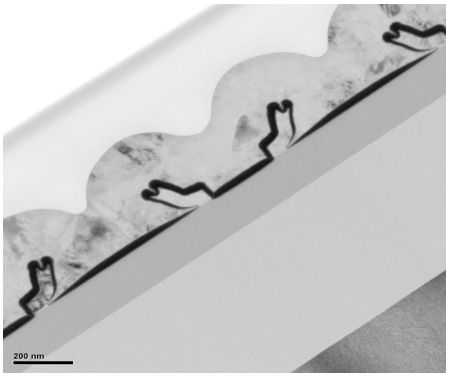

Fig 3. The cross-section transmission electron microscope (TEM) microphotograph of the FL-TFTs.

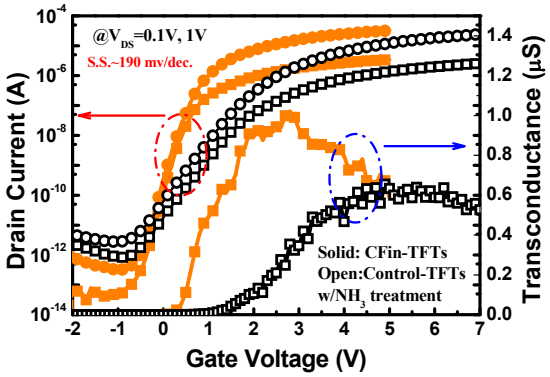

Fig 5. The I_D-V_G characteristics of FL-TFTs and Control-TFTs, respectively.

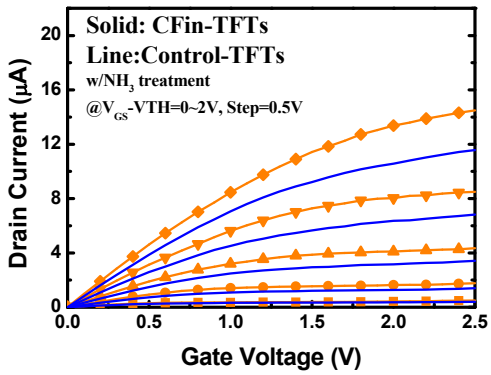

Fig 7. The output characteristics of FL-TFTs and Control-TFTs, respectively.

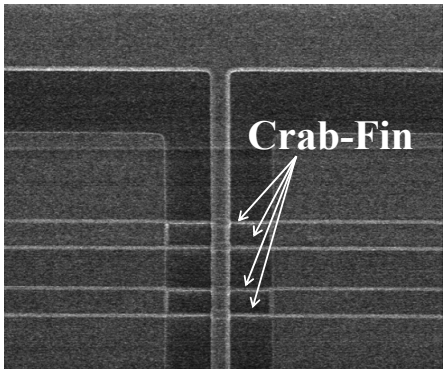

Fig 2. The scanning electron microscope (SEM) microphotograph of the FL-TFTs. The gate length is 0.35 μm.

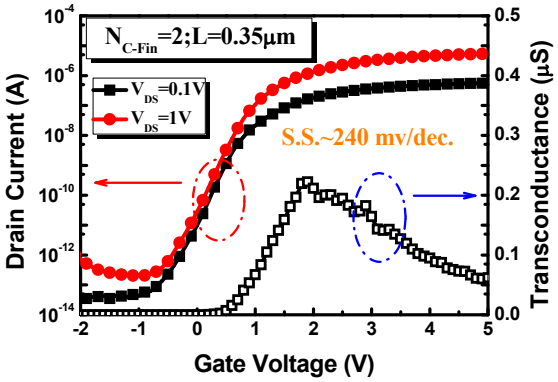

Fig 4. The I_D-V_G characteristics of FL-TFTs.

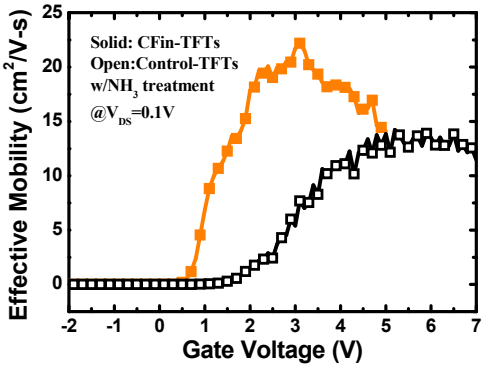

Fig 6. The effective mobility of FL-TFTs and Control-TFTs, respectively.

	This Work	Ref. A	Ref. B	Ref. C		Ref. D
Structure	CFIN-TFTs	HM-TFTs	HM-TFTs	Dual Gate	Single Gate	DSSB
Channel	SPC	SPC	SPC	HRELC		SPC
Gate Stack	Poly-Si / SiO_2	TaN / $HfSiO_X$	Poly-Si/ HfO_2	Poly-Si / SiO_2		Poly-Si / SiO_2
W/L (μm/μm)	0.7*/0.35	150/0.3	0.1/1	3/4		0.05/0.14
VTH (V)	0.5	0.75	0.3	1.57	2.17	N/A
EOT (nm)	15	2.8	2.7	100	100	5
S.S. (mv/dec.)	190	193	280	550	790	215
I_{ON}/I_{OFF} (V_{DD})	~10^8 (1V)	>10^6 (1V)	9.7x10^6 (1V)	>10^7 (10V)	>10^7 (10V)	~10^6 (-1V)

Table 1. Comparison of important parameters from this work to other published results. [A] M. H. Lee et al. SSDM, pp1036-1037,2009. [B] C.-P. Lin et al., EDL, vol. 27, no. 5, pp. 360–363, May 2006. [C] Po-Tsun Liu et al. EDL, vol. 28, no. 8, pp. 722–724, 2007. [D] Sung-Jin Choi, et al., EDL, vol. 31, no. 3, p. 228-230, 2010.