Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp187-188

Enhancement of Stress Memorization Technique (SMT) by High Thermal Annealing Temperature

Hsu-Yu Chang and Jason C.S. Woo
Electrical Engineering Department
University of California, Los Angeles
Los Angeles, CA90095
Tel: +1-310-206-7331 Email: cursive@ucla.edu

Abstract - In this paper, different annealing temperature at gate memorizing strain step is studied. Device performance shows SMT device with higher annealing temperature (1150°C) can induce more strain memorized in the gate. The experimental data of SMT device with higher annealing temperature shows significant improvement of electron mobility compared to lower annealing temperature (1000°C).

1. Introduction

Strain is known to improve carrier mobility and boost device performance [1]. Uniaxial strain is widely used in CMOS technology, such as compressive strain from epi SiGe on PMOSFET and tensile strain from the deposition of tensile SiN on NMOSFET [2]. In addition, another technology, stress memorization technique(SMT), is proven to induce the strain without any tensile layer on device. This SMT device combined with additional tensile layer can have further improvement of device performance [3]. However, the relation between annealing temperature and the gate with memorizing strain is still unknown.

In this work, the SMT devices with different RTA annealing temperature at gate memorizing step are studied. The experimental SMT device characteristics are also shown in this paper.

2. Device Fabrication

Fig. 1 shows the process flow in this work. P-type SOI wafers with 50nm thickness are used in this process. After LOCOS isolation, 3nm gate oxide is grown and followed by 100nm LPCVD poly-Si deposition. Then wafers are implanted with As which can partly amorphize poly gate. LPCVD SiN is deposited on poly-gate, and wafers are annealed by RTA for stress memorization in poly gate. After removing SiN by wet etch, the wafers are followed by LTO deposition to prevent the gate amorphized during S/D implantation, gate definition, LDD, spacer formation, deep source/drain implantation and activation. Finally, NiSi is formed in source/drain region to reduce series resistance.

3. Experimental Results and Discussion

Fig. 2 shows the SiN thickness with different intrinsic stress. Higher stress can induce more strain in the poly gate. As SiN thickness increase, the intrinsic stress is accumulated, but reaches a saturation value (~1 GPa) after 100nm. In order to check the stress in SiN after high temperature annealing (1150°C), the test wafer with 100nm SiN is used to measure the stress change by curvature measurement. The SiN stress with RTA annealing (1150°C) is about 970M Pa, and there is no significant change of intrinsic stress.

Fig. 3 shows the I_D-V_D measurement with stress memorization technique at different RTA temperature. From the figure, the device with higher annealing temperature (1150°C) has better current performance than the device with lower annealing temperature (1000°C). By memorizing the strain from SiN and the re-crystallization of poly, poly gate exhibits vertical tensile strain. This induces not only a vertical compressive strain, but also horizontal tensile strain along the channel. This tensile strain along the channel can reduce carrier scattering and improve electron mobility [4]. Because SiN has larger thermal expansion coefficient than poly-Si, high temperature annealing process will induce more strain between these two layers [5]. Hence, device with higher temperature annealing (1150°C) results in more tensile strain inside the channel. The relation between annealing temperature and strain effect is demonstrated in Fig. 4. The higher temperature annealing process will induce more strain in the poly and also channel.

Fig. 5 shows the mobility of these two devices(Lg = 0.23um) with different SMT annealing temperatures. As indicated in the figure, the SMT device with higher RTA annealing has larger mobility. The mobility has significant improvement (200~300% higher than the SMT device with 1000°C annealing process). It proves that the higher temperature can induce more tensile strain along the channel.

Fig. 6. plots mobility improvement with different channel length. It shows that the mobility improvement decreased with longer channel length. The mobility improves from 200~300% in SMT device with 0.23um channel length to 0 % in SMT device with 1.2 or 2.2 um channel length.

Fig. 7. shows the transconductance with different channel length. SMT device with short channel length has higher transconductance and it is about 200% higher than the device with low RTA annealing temperature.

4. Conclusion

This work explores the relation between thermal annealing temperature and stress memorization in poly gate. From our results, the SMT device with higher annealing temperature (1150°C) for poly-gate to memorize the strain has significant mobility improvement (200~300%), and transconductance also has obvious enhancements (~200%).

This relates to different thermal expansion properties between SiN and poly, and the recrystallizaiton of poly. This strain effect decreases with the longer channel length.

Reference

[1] T. Ghani, et. al., IEEE Electron Devices Meering(IEDM), (2003), 978.

[2] S. E. Thompson, et. al., IEEE Electron Devices, 51, (2004), 1790.

[3] C. H. Chen, et. al., Symposium on VLSl Technology Digest of Technical Papers, (2004), 56

[4] C. Ortolland, et. al., IEEE Electron Devices 56, (2009) 1690.

[5] N. Serra, et. al., IEEE Electron Devices Meering(IEDM), (2009), 71.

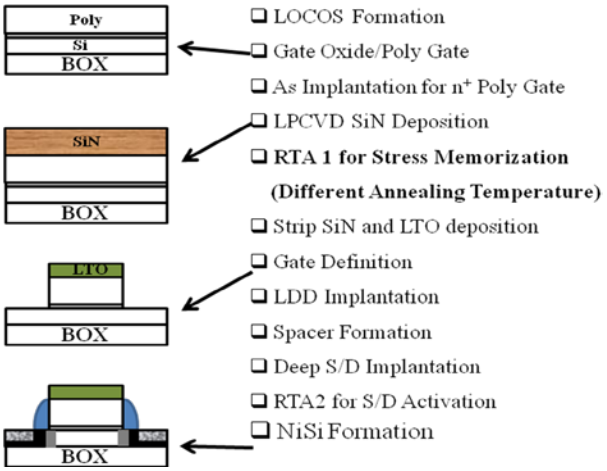

Fig. 1 Process flow of this work.

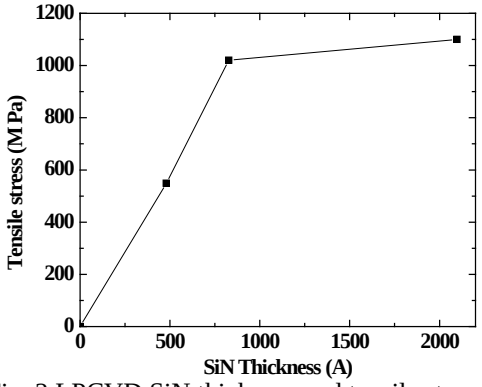

Fig. 2 LPCVD SiN thickness and tensile stress.

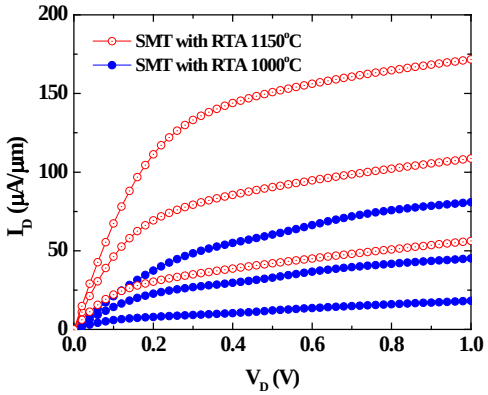

Fig. 3 I_D-V_D relation of two SMT devices(Lg=0.23um) with different RTA temperature at V_G-V_T=0.15, 0.3, 0.45 V.

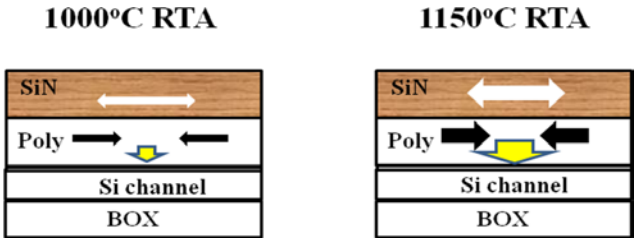

Fig. 4 The strain distribution at different RTA temperatre.

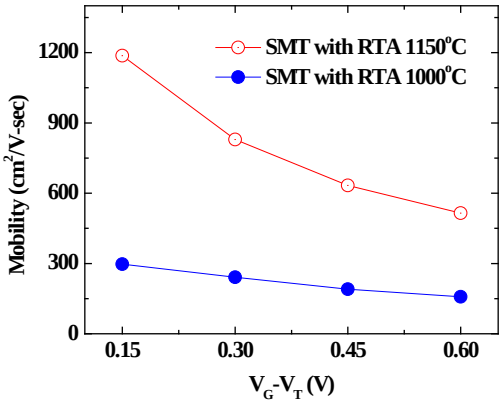

Fig. 5 Mobility of SMT devices(Lg=0.23um) with different RTA temperatures.

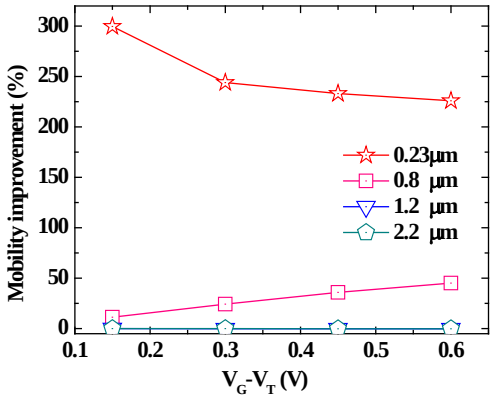

Fig.6 Mobility improvement of SMT device with 1150°C annealing temperature device at different channel length.

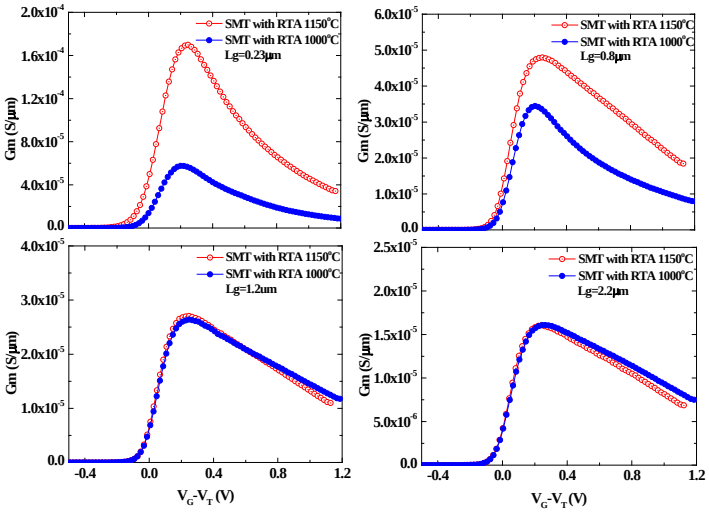

Fig. 7 Transconductance of SMT with different RTA temperatures at different channel length at V_D=0.1V.