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Fabrication of hp 25nm Si Pillar Using New Multiple Double Patterning Technique

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1. Introduction

As the continuous shrinkage of ULSI device going on, fabrication of conventional planar type device had come to meet great difficulties such as limitation of photolithography. To overcome this problem, pillar type cell device structures were proposed [1,2]. It becomes possible to fabricate more high-density cells using vertical structure compared with the conventional planar type devices without increasing chip area. For the production of these 3D devices, it is indispensable that the verification of vertical Si pillar fabrication techniques. In this paper, we proposed new fabrication technology of slim silicon pillar with multiple double patterning technique. Moreover, we have confirmed that by using proposed multiple double patterning technique, the formation of Si pillars of 23.6nm with the pitch of 50nm can be realized on 300mm wafer, using line and space photolithography with 100nm pitch (i.e. 50nm in half pitch)

2. Double patterning technique

The process flow of proposed multiple double patterning technique is shown in Fig. 1. 100nm thick Si_3N_4 and amorphous Si film was deposited on Si substrate by thermal chemical vapor deposition. First photo-resist pat-tern was formed with 50nm half pitch line and space by 193nm H_2O immersion exposure system (NA=1.35). We have applied double patterning technique [3] to this photo-resist pattern and formed 25nm half pitch line and space pattern. At first, photo-resist line width was shrunk from 50nm to 25nm by reactive ion etching process. Then inorganic film, which forms sidewall spacer, was deposited on photo-resist directly under ultra-low process temperature so that photo-resist pattern does not shrink by deposition process. Using photo resist as core, material can be effective in significantly decreasing in double patterning costs. 25nm half pitch line and space mask was formed by etch-back of inorganic film and the photo-resist core removal by in-situ ash process in the etcher. After etching of amorphous Si layer and removal of inorganic mask by wet cleaning, optimized organic material was buried into the first high-aspect line and space pattern. Second line and space photolithography was then performed so that first amorphous Si line and second photo-resist line crossed each other. By repeating double patterning process to the second photo-resist pattern, the amorphous Si mask pattern for the dense pillars with 50nm pitch was formed. Since angular shaped mask is rounded during Si_3N_4 layer and substrate Si etching, dense cylindrical Si pillars with the pitch of 50nm were finally fabricated on 300mm wafer.

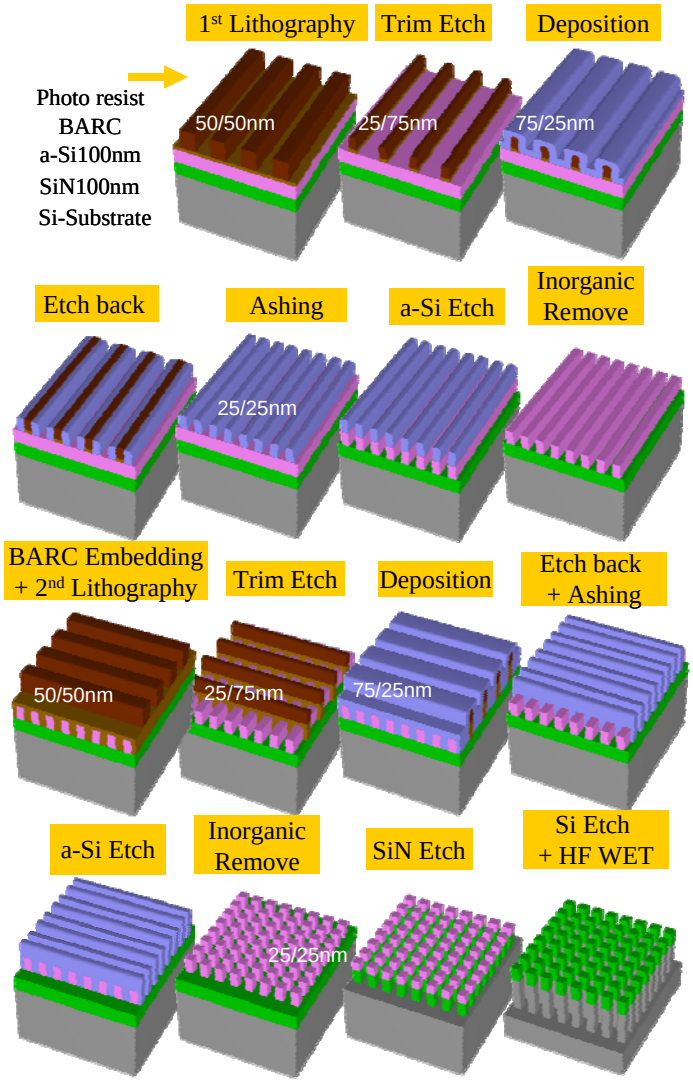


Fig. 1 Cross pattern with side wall transfer process flow of 50nm pitch Si pillar fabrication

SEM images of fabricated Si pillars are shown in Fig. 2. The height of the pillar was 110nm at the center of the 300mm wafer and 115nm at the edge. The top view of fabricated Si pillars is evaluated by SEM as shown in Fig.3.

As shown in Fig.3, the diameter of the fabricated Si pillars is 23.6nm and its pitch is 50nm.We have also measured the top diameter of pillar by CD-SEM and result is shown in Fig. 4. The average diameter of the fabricated Si pillars is 23.6nm and its 3 sigma within 300mm wafer was only 1.7nm.

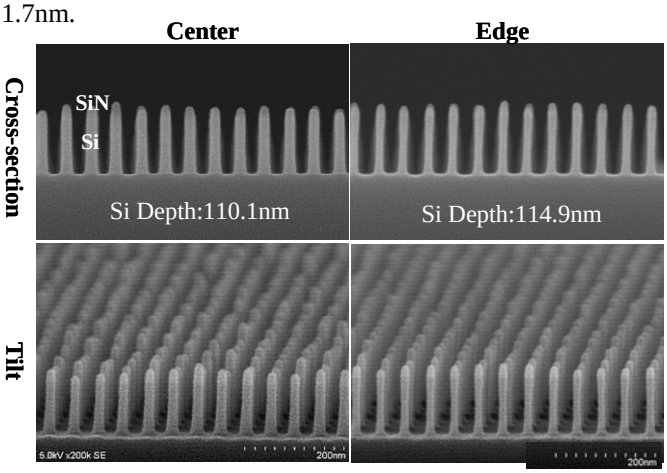


Fig. 2 SEM images of fabricated 50nm pitch Si pillar

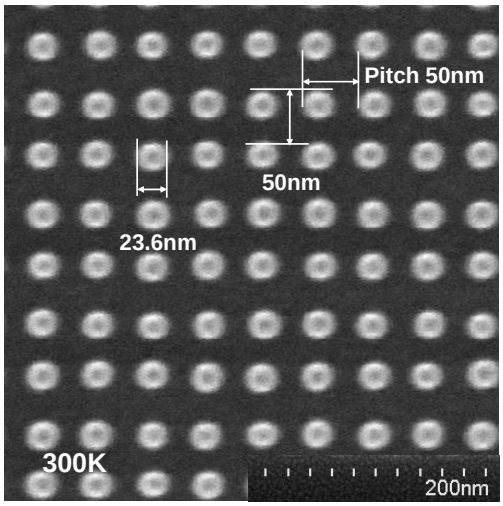
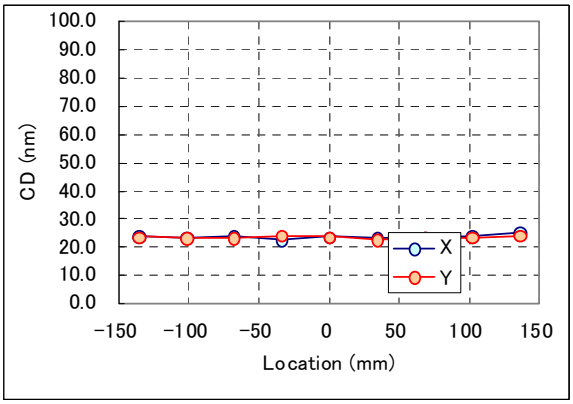


Fig. 3 Top view of fabricated Si pillars



CD(Ave):23.6nm
3σ:1.7nm

Fig. 4 Top diameter of fabricated Si pillar within 300mm wafer measured by CD-SEM.

From above all, it is confirmed that by using proposed multiple double patterning technique, the formation of Si pillars of 23.6nm with the pitch of 50nm can be realized on 300mm wafer, using line and space photolithography with 100nm pitch (i.e. 50nm in half pitch)

3. Advanced Si etching by capacitive coupled plasma

To achieve preferable profile in Si pillar etching, we have used low-density plasma etcher so that the number of ions does not increase so much. To secure the margin of etch profile control and etch uniformity within wafer, quick exhaust of the byproduct of Si etching from the chamber is required so that re-deposition is minimized. On the other hand, higher discharge pressure is preferable to achieve high etch rate and stable discharge. Thus it is preferable to select the plasma source that can achieve uniform and relatively low plasma density even with small chamber volume. For this reason, we have adopted narrow gap capacitive coupled plasma (CCP) etcher in this fabrication procedure.

4. Conclusions

Novel method to fabricate 50nm pitch dense Si pillar that would apply to the fabrication of vertical cell devices was developed. By using proposed multiple double patterning technique, the hp25 Si pillar etching profile has enough uniformity in 300mm wafer. The authors are currently engaged in further investigation of Si pillars fabrication technique.

5. Acknowledgements

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