Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp199-200

In-situ Formation of HfN/HfSiON Gate Stacks with 0.5 nm EOT Utilizing ECR Sputtering on Three-Dimensional Si Structures

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1. Introduction

Metal/high-k gate stacks are necessary even for three-dimensional (3D) gate MOSFETs for continued scaling [1]. Atomic layer deposition (ALD) is a conventional method for high-k deposition; however, it still has some difficulties because of the contamination caused by the residues of the precursor source gases generally degrades the leakage properties [2].

In this study, *in-situ* formation of HfN/HfSiON gate stacks on the 3D Si structures were investigated utilizing ECR plasma sputtering which is a low-damage process, and is expected to form excellent films [3].

2. Experimental Procedure

MIS diodes on planar and 3D Si structures were fabricated with the process flow shown in Figure 1. Narrow line (0.4 – 9.3 μm) patterns were fabricated using 1 - 10 μm line and space (L&S) masks on p-Si(100) by a g-line stepper. Dry etching (10 nm) was carried out by ICP-RIE. The wafers were chemically cleaned followed by the annealing at 1000°C for 1 min in N_2 ambient for the retrieval of the etching damage. Next, the chemical oxide (C'O) layers (0.7 nm) were formed by H_2O_2 solution. Then, HfN (1 nm) was deposited by ECR sputtering at 0.19 Pa (Ar/N_2 flow rate of 25/1 sccm) followed by the *in-situ* oxidation at 0.18 Pa (Ar/O_2 flow rate of 20/8 sccm) for 3 s. After *in-situ* oxidation, HfN (50 nm) was deposited *in-situ* (Ar/N_2 flow rate of 20/0.8 sccm). Post deposition annealing (PDA) was performed by silicon-wafer-covering rapid thermal annealing (SWC-RTA) at 400-900 °C for 15 s in N_2 ambient [4]. For the gate electrode formation, HfN was selectively etched by $HF:H_2O_2:H_2O=1:2:40$ [5]. Finally, the Al electrodes were evaporated on the back side. The fabricated MIS diodes were characterized by capacitance-voltage (C-V), current-voltage (J-V) methods and cross-sectional scanning electron microscopy (SEM). The EOTs were evaluated using EPOQUE with quantum mechanical correction [6], and the conductance method was performed to determine the density of interface states (D_{it}). Schematics and cross-sectional SEM image of the MIS diodes were shown in Figure 2, respectively.

3. Results and Discussion

Figure 3 shows the PDA temperature dependence of C-V characteristics of planar HfN/HfSiON/p-Si(100) gate stacks. From C-V characteristics, the EOTs of 0.5 - 0.58 nm were obtained. As shown in Figs. 3(c) and 3(d), remarkable frequency dispersion was observed with PDA temperature. Figure 4 shows D_{it} and hysteresis widths as a function of PDA temperature. As shown in Fig. 4, D_{it} of HfN/HfSiON/p-Si(100) annealed at 550-600ºC was as low as an order of 10^{11} $cm^{-2}eV^{-1}$ while the hysteresis width increased as the PDA temperature decreased. From these results, it was suggested that high temperature PDA causes a reaction at the interfaces of HfN/HfSiON and/or HfSiON/p-Si(100). Figure 5(a) shows the PDA temperature dependence of EOT and leakage current at V_{FB}-1 V. From Fig. 5(a), the EOT of 0.5 nm and leakage current of 1.3 A/cm^2 at V_{FB}-1 V were obtained at the PDA temperature of 600ºC. As shown in Fig. 5(b), the leakage current was lower than FUSI-NiSi/HfO_2/$HfSiO_x$-IL/p-Si(100) [7]. It might be due to the *in-situ* formation of metal gate and/or suppression of oxygen vacancy by N atoms. From these results, it can be said that 600ºC is a suitable condition for PDA.

Next, the HfN/HfSiON gate stacks on 3D Si structures with the PDA temperature of 600ºC were investigated. Figure 6 shows the C-V and J-V characteristics of gate stacks on 3D Si structures. Figure 7 shows line width dependence of leakage currents at V_{FB}-1 V. As shown in Fig. 6(a), C-V characteristic with small hysteresis and negligible frequency dispersion was obtained even on 3D Si structures. As shown in Fig. 7, the gate leakage current for 0.4 μm line degraded about 3 orders of magnitude compare to 9.3 μm line, although the difference in the line widths was an order of magnitude.

4. Conclusion

In-situ formation of HfN/HfSiON gate stacks by ECR sputtering was investigated. Annealing temperature was important parameter and the temperature of 600ºC is suitable to suppress the D_{it} and the frequency dispersion. It was found that *in-situ* formed HfN/HfSiON gate stacks realize ultra-thin EOT and low leakage current even on 3D Si structures.

Acknowledgements

The authors would like to thank Profs. H. Ishiwara, H. Iwai and Y. Higo, Dr. K. Kakushima and Mr. N. Hatakeyama of Tokyo Institute of Technology, Dr. Y. Jin of NTT and Drs. M. Shimada and K. Saito of MES-Afty for their support and useful discussions for this research.

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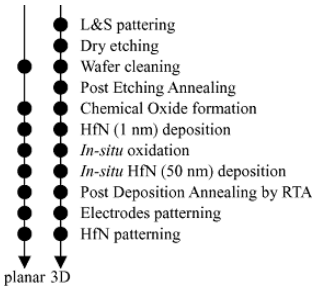


Fig. 1 Process flow.

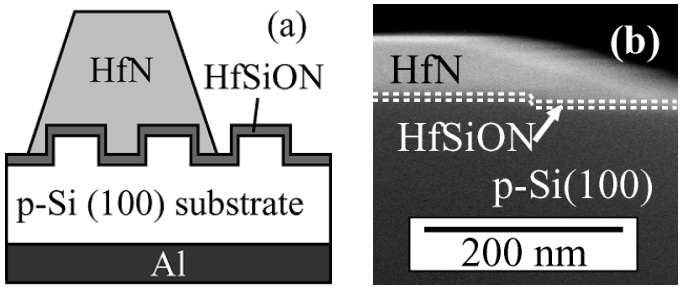


Fig. 2 (a) Schematic and (b) SEM image of fabricated 3D MIS diode.

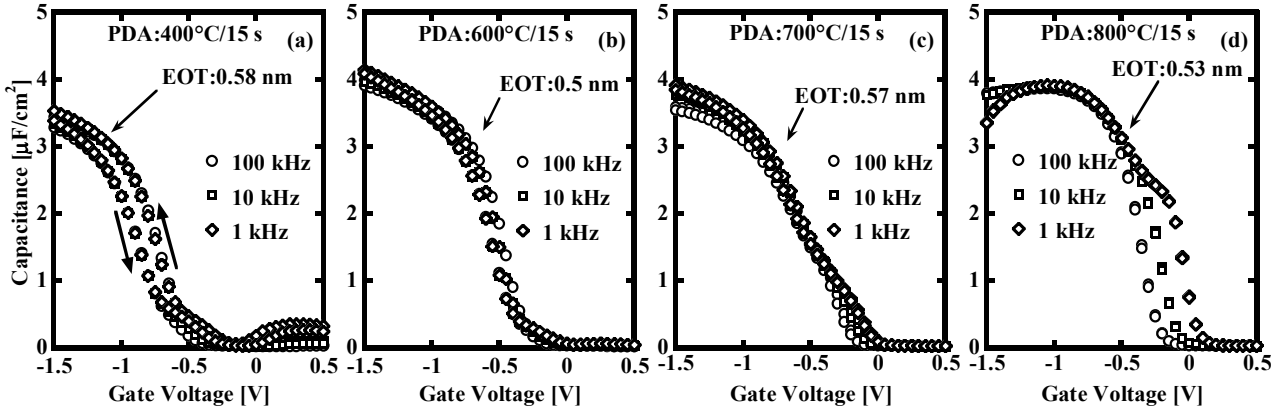


Fig. 3 PDA temperature dependence of C-V characteristics of planar HfN/HfSiON/p-Si(100) gate stacks PDA temperatures are (a) 400ºC, (b) 600ºC, (c) 700ºC, and (d) 800ºC.

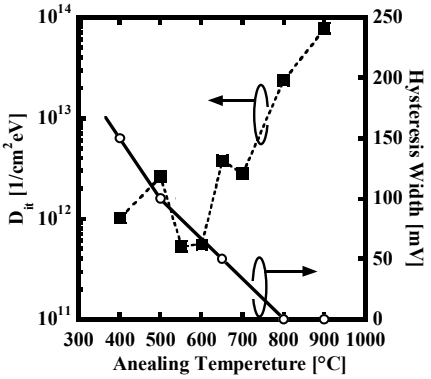


Fig. 4 D_{it} and Hysteresis width of deferent PDA temperature.

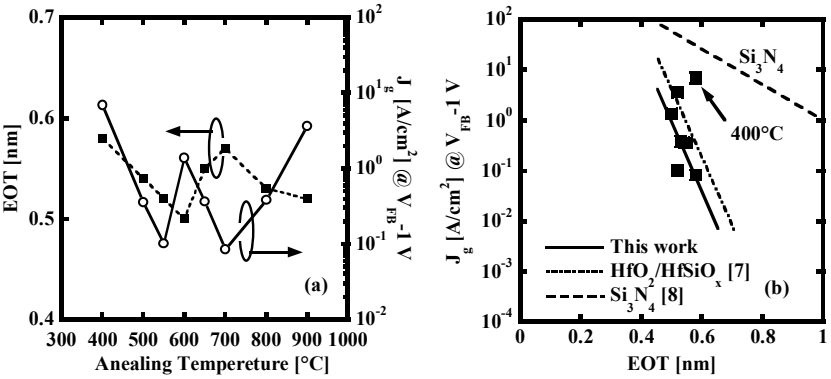
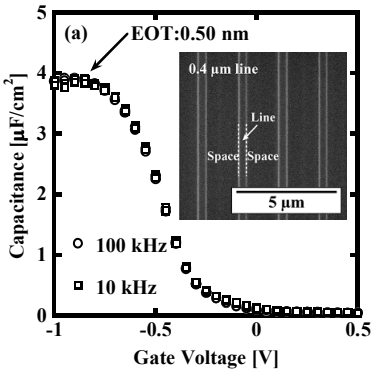


Fig. 5 (a) PDA temperature dependence of EOT and leakage current at V_{FB}-1 V (b) EOT versus current densities plot.



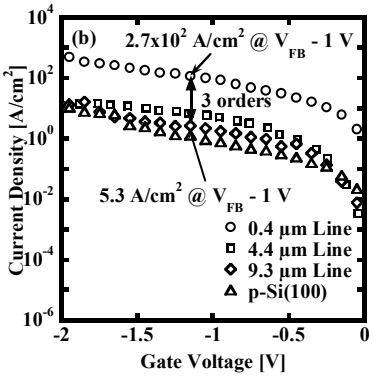


Fig. 6 (a) C-V and (b) J-V characteristics of HfN/HfSiON gate stacks. on 3D Si structures.

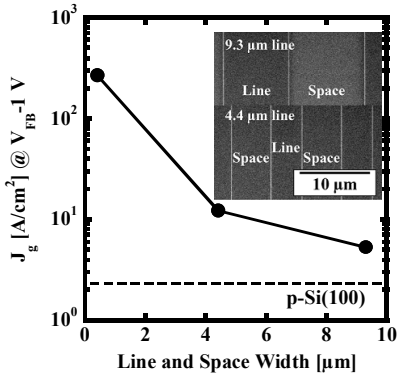


Fig. 7 Line width dependence of J-V characteristics.