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# Power-Aware Bit-Serial Binary Content-Addressable Memory Using Magnetic-Tunnel-Junction-Based Fine-Grained Power-Gating Scheme

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## 1. Introduction

Content-addressable memories (CAMs), that are high-speed parallel data search engines [1], have two major problems in power dissipation as well as bit-cell cost. As one of the promising candidates of low-power and compact hardware realization, novel circuit architectures, called MOS/Magnetic-Tunnel-Junction (MTJ)-hybrid nonvolatile logic-in-memory, have been reported [2-6]. In this paper, we present an ultra-low-static-power bit-serial binary CAM using an MTJ-based fine-grained power-gating scheme. Since a single MTJ device is used as not only a nonvolatile storage element, but also a logic-operation element, one-transistor/one-MTJ (1T-1R)-style CAM cell circuit is implemented. A nonvolatile storage capability is very suitable for realizing power-gating mechanism. As a result, most of static power is eliminated with activity rate of 1.55 percent using fine-grained power-gating.

## 2. Advantages of MOS/MTJ-Hybrid Logic-in-Memory Circuitry

Fig. 1 shows a structure and a symbol of an MTJ device, whose structure consists of a synthetic ferrimagnetic (SyF) free layer, an MgO tunnel barrier, and a fixed layer [3-5]. According to the spin (magnetization) direction of the free layer with respect to that of the fixed layer, there are two distinct states as the different resistances of the MTJ device; low resistance $R_P$ when the spin directions are parallel and high resistance $R_{AP}$ when anti-parallel. Thus, the MTJ device can be considered as a variable resistor, which indicates that the MTJ device has not only nonvolatile storage capability but also pseudo switching capability to build a logic device in accordance with stored data. A nonvolatile storage function and a logic function are merged into an MTJ device in the nonvolatile logic-in-memory circuit and the stored logic value does not disappear even if power supply is cut off. Therefore, it is not required to write/read to/from MTJ devices before/after power-off/power-on, which results in realizing quick sleep/wake-up behavior and low power dissipation in the VLSI chip as shown in Fig. 2.

## 3. Bit-Serial Binary CAM Based on 1T-1R Cell and Fine-Grained Power-Gating Scheme

Fig. 3 shows an overall structure of the proposed bit-serial binary CAM, which consists of several parts; word circuits including a CAM cell array, sense amplifiers (SAs), accumulators (ACCs), and peripheral circuits such as search-line, word-line, bit-line, and output drivers. The word-parallel bit-serial equality-search operation between a search word (input key) and every word stored into the CAM cell array is performed. The bit-level search result of the each linear array of CAM cells is amplified by the corresponding SA, and accumulated by the corresponding ACC. Since the ACC remains the initial state as long as the result of the bit-level search is matched, the final result of the word circuit can be detected by the state of the ACC.

Fig. 4(a) shows a conventional CMOS-based 9T binary CAM cell. Since a volatile storage element (SRAM cell) and a comparison circuit are separated in the CMOS-based CAM cell, its cell size and static power become large. On the other hand, the proposed MOS/MTJ-hybrid 1T-1R binary CAM cell in Fig. 4(b) merges comparison logic and nonvolatile storage functions compactly by using MOS/MTJ-hybrid logic-in-memory circuit structure, which can operate with low power dissipation.

In order to realize a compact and nonvolatile binary CAM cell, we focused on the amount of resistances of the MOS device and the MTJ device in the cell. Fig. 4(c) shows a truth table of the proposed binary CAM cell. In this figure, the cell resistances in accordance with the stored data and the input data are also indicated. As shown in Fig. 4(d), the cell resistance consists of only three states by adjusting input voltage $V_{SL}$ in order that $R_P+R_H=R_{AP}+R_L$. The three-valued resistances can be detected by an SA during the equality-search operation. In this way, internal three-valued logic is utilized in our binary CAM cell design with maintaining operating margin compared to a binary-logic implementation, while the binary-logic-based CAM cell requires twice number of devices, because complementary storage data and input data are used for comparison logic.

Fig. 5 shows the proposed word circuit with a fine-grained power-gating capability. Whenever a new input key is applied and the new equality-search operation is performed, the output of the word circuit is initialized to a high voltage level by controlling the INIT signal, while the PMOS power switch PS is also turned on. The equality-search operation is parallel by word and serial by bit-slice. In each cycle, a bit-level equality-search operation on a single bit-slice is performed. While an input bit is continuously equal to the corresponding stored bit, the output from the SA remains a high voltage level. Once a mismatched result between an input bit and a stored bit is detected in a sequence of bit-level equality-search operations, the output from the SA becomes a low voltage level. As the result, the output from the ACC also becomes a low voltage level, while the SLEEP signal becomes a high voltage level to cut off the power switch. From then on until the next input key is applied, the power supply of the word circuit (except the ACC) is cut off in order to suppress static power dissipation. The power gating makes it easily possible to turn off the power switch PS because there is not a power-supply line in the linear array of the proposed CAM cells as shown in Fig. 4(b) and the MTJ devices have nonvolatile storage capability. In the case of a CMOS-based CAM cell, the power supply can not be cut off even if they are in a standby mode, because stored data must be maintained in volatile memory elements (SRAMs). The data is written into each MTJ device in advance by activating the write enable signal, WE, word-line signals, WLs, and dual-rail bit-line signals, BL and BL'.

Fig. 6 shows an example of fine-grained power-gating behavior in the 3-bit x 8-word bit-serial CAM. In the first-bit search operation on the first bit-slice, the input bit is applied to all CAM cells on the bit-slice, which results in mismatch in the four rows of the word circuit. In the second-bit search operation, the input bit is applied to all CAM cells on the second bit-slice. During the second-bit search operation, the four rows of the CAM cells and SAs are in a standby mode by the power gating, while the additional mismatch in the two rows of the word circuit are detected. In the third-bit search operation, the number of circuit blocks in a standby mode increases in the same way. According to the word length of the proposed CAM, the effectiveness of the static-power reduction by the fine-grained power-gating is increased.

## 4. Evaluations and Conclusions

Table I summarizes the comparison of the static power dissipations between a conventional CMOS-based bit-serial CAM cell array and the proposed one. The CMOS-based

CAM cell array constantly consumes static power in the volatile storage elements (SRAMs).

On the other hand, the proposed CAM cell array can suppress static power dissipation because of the nonvolatile capability and the fine-grained power management of them. As the result, it is evaluated that most of the static power dissipation of the proposed CAM cell array is eliminated with activity rate of 1.55 percent under a 90nm CMOS/MTJ technology.

From these points of view, it is expected that the MOS/MTJ-hybrid nonvolatile login-in-memory circuitry with a fine-grained power-gating capability is one of the most effective methods to overcome a static power problem.


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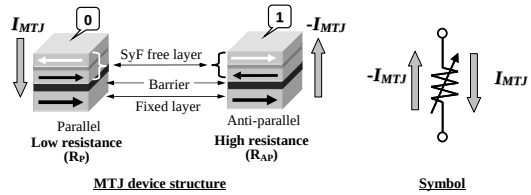


Fig. 1 MTJ device structure and symbol.

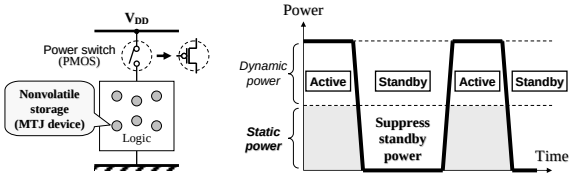


Fig. 2 Power gating in a nonvolatile logic-in-memory system.

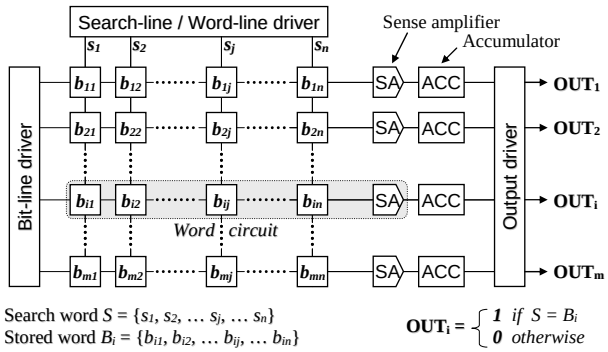


Fig. 3 Overall structure of the proposed bit-serial CAM.

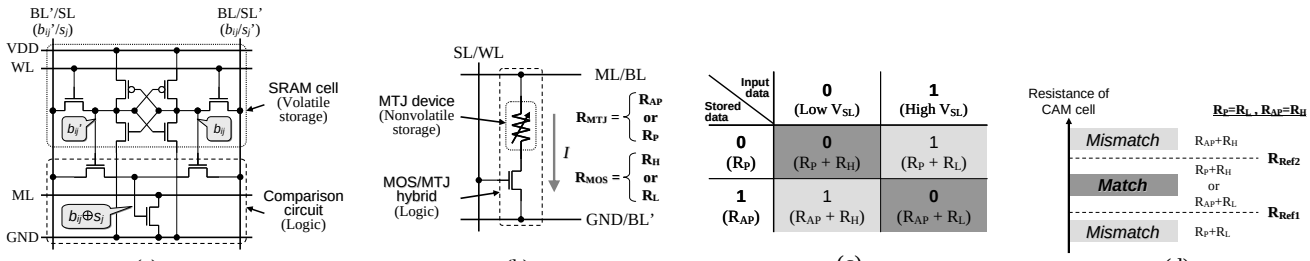


Fig. 4 Binary CAM cells; (a) Conventional 9T cell, (b) Proposed 1T-1R cell, (c) Truth table, (d) Resistances of the proposed cell.

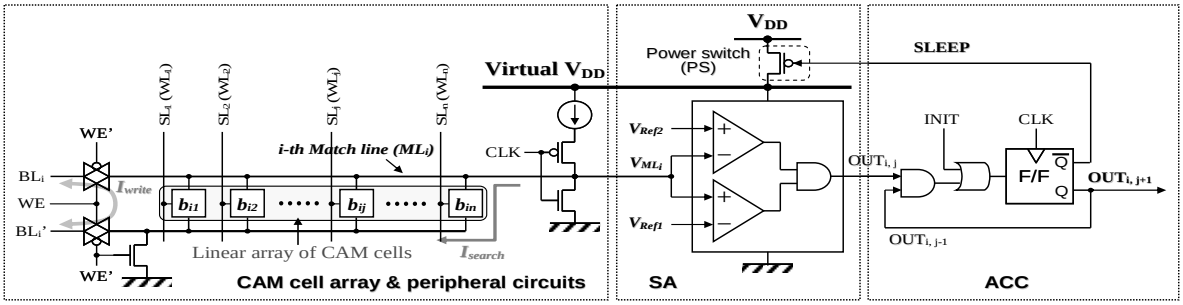


Fig. 5 The proposed word circuit with fine-grained power-gating capability.

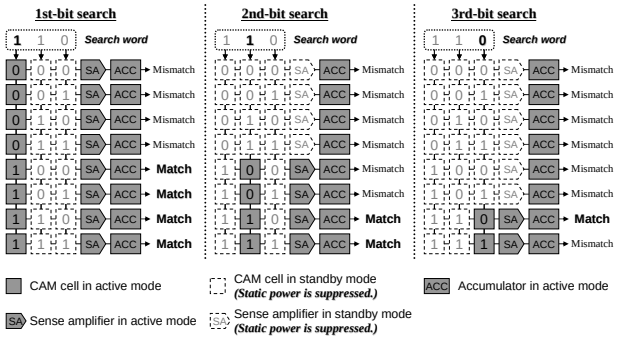


Fig. 6 Fine-grained power gating in the proposed bit-serial TCAM.

Table I Comparison of static power dissipations in 128-bit x 256-word bit-serial CAM cell arrays.

| | | **Conventional** (without power gating) | **Proposed** (with power gating) |
|---|---|---|---|
| **Activity rate [%]** | | 100 | **1.55** |
| **Static power [μW]** | Storage elements in CAM cell | 267.3 (@SRAM cells) | **0 (@MTJs)** |
| | Logic elements in CAM cell | 64.2 (@XOR circuits) | **0.00179 (@MOS/MTJ-hybrid XOR circuits)** |
| | Total | 331.5 | **0.00179** |

HSPICE simulation under a 90nm CMOS/MTJ technology, $V_{DD}$=1.2V