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Performance Comparisons of Schottky Barrier Transistors Using Si-, Ge- and Ge-Si Core-Shell Nanowires as Channels

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1. Introduction

With the scaling down of transistor feature size to several *deca*-nanometer regimes, silicon nanowire (Si-NW) as device channel and metal/silicide as source/drain are two promising candidates for future structure [1-4]. Si-NWs have excellent intrinsic electrostatics and transport properties [1, 2], while silicide source/drain structure can achieve low series resistance and low thermal budget [3, 4]. Therefore, Schottky barrier silicon nanowire transistor (SB-Si-NWT) is designed to take advantage of both structures [5]. On the other hand, Ge has been regarded as a replacement for silicon channel in high-speed applications for its much higher mobility [4]. But there are few reports about Ge-NWT due to the difficulties in real fabrications. And Ge-Si core-shell nanowire (CS-NW) structure is thus developed and experimentally prepared as a substitute to make use of the high mobility vantage of Ge material in nanowire technologies [6].

In this paper, the performance of SB-Si-NWTs, SB-Ge-NWTs, and SB-CS-NWTs are simulated with 3D device simulator Synopsys Sentaurus TCAD tools, and the major impact factors on the device characteristics are discussed.

2. Device structure and working mechanism

The schematic structures of the SB-Si-NWT, SB-Ge-NWT, and SB-CS-NWT for the simulations are illustrated in *Fig*.1. The gate length, L_g, ranges from 10 to 25nm; the nanowire radius, R, ranges from 3 to 6nm; and the equivalent gate dielectric thickness, T_{ox}, is 1nm. Undoped *p*-channel transistors are focused in our simulations. The supply power voltage, V_{dd}, is -0.5V. Silicide Schottky barrier height (*Si-SBH*) for holes ranges from 0 to 0.3eV, with 0.2eV as default (suggesting PtSi), and germanide Schottky barrier height (*Ge-SBH*) for holes ranges from 0 to 0.2eV, with 0.1eV as default (suggesting PtGe). The tunneling mass and mobility of Ge material is set according to the calibration on planar Ge SB-*p*MOSFET, which is well-fitting to the experimental data [4] as shown in *Fig*.2.

There are several works on the mechanism of SB-Si-NWT [5], but the transport characteristic of SB-CS-NWT is still not clear. Here, *Fig*.3 shows the electrostatic potential and hole current density of the cross section along SB-CS-NWT's channel. In *Fig*.3(a), the potential change rate at the source side (at x=12.5nm) near the Ge/Si heterojuctions (at y=-3 and 3nm) is the highest, which results in the thinnest barrier and the highest tunneling probability. From *Fig*.3(b), it can be found that hole current concentrates in Ge channel near the heterojuctions due to its much higher hole mobility than Si.

3. Results and discussions

The transfer curves of SB-Si-NWT, SB-Ge-NWT, and SB-CS-NWT are simulated in *Fig*.4. The drain current of each device is normalized by being divided by the perimeter of nanowire on account of the all-around gate, and the gate work function is tuned to fix Ioff at 10^{-7}A/um for each device.

Fig.5 shows I_{on}-R as well as I_{on}-R_c relationships, in which R varies from 3 to 6nm (for SB-Si-NWTs and SB-Ge-NWTs) and R_c is either fixed at 3nm or varies with R to keep R-R_c=2nm (for SB-CS-NWTs). SB-CS-NWT provides larger I_{on} than the others. With R decreasing, the drivabilities of all devices are enhanced, except for the SB-CS-NWTs with R_c decreasing simultaneously, because the sectional area of Ge core is diminished. *Fig*.6 shows relationship between sub-threshold slope (*SS*) and *R*. *SS* of SB-Si-NWT and SB-CS-NWT is smaller than that of SB-Ge-NWT's and decreases when R decreases.

Fig.7 plots the relation between I_{on} and R_c with different R. It can also be found that larger R_c and smaller R can generate larger I_{on}. In *Fig*.8, the influence of *Si-SBH* on I_{on} is studied. Lower *Si-SBH* can greatly improved I_{on} of SB-Si-NWT, but I_{on} of SB-CS-NWT is less sensitive to *Si-SBH*. Another simulation result shown in *Fig*.9 suggests that *SS* of SB-Si-NWT will increase rapidly when *Si-SBH* is larger than 0.2eV, and SB-CS-NWT is still insensitive to *Si-SBH*. In *Fig*.10, we can see that lower *Ge-SBH* enhances I_{on} of both SB-Ge-NWT and SB-CS-NWT.

The relation between *SS* and L_g with different R is simulated in *Fig*.11. For all structures, smaller R can lower *SS* when L_g is scaled down. Besides, SB-Si-NWT has the lowest *SS*, and *SS* of SB-CS-NWT is lower than SB-Ge-NWT's with smaller R.

4. Conclusions

We have simulated and studied the characteristics of SB-Si-NWT, SB-Ge-NWT, and SB-CS-NWT respectively. Generally speaking, SB-Si-NWTs have the lowest *SS*, while SB-Ge-NWTs obtain the highest I_{on}. It's found that decreasing nanowires' radius helps to enhance device performance. For SB-CS-NWT, most holes tunnel at the source near the heterojuction and transport in the Ge core region. It's also noticed the drivability of SB-CS-NWT is relatively insensitive to SBH of source/drain contact, which will bring benefits for selection of source/drain materials.

Acknowledgements

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References

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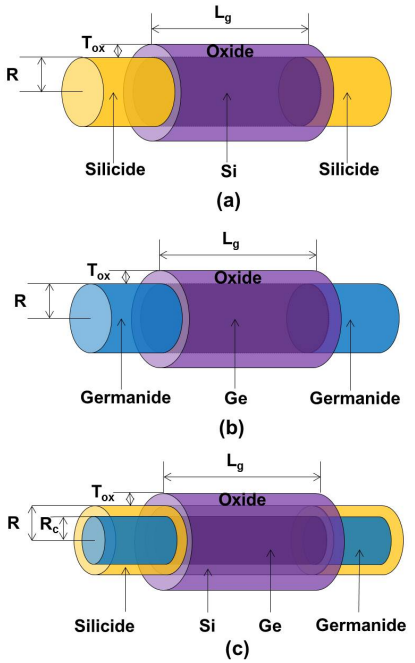

*Fig.*1 Schematic structure of (a) SB-Si-NWT, (b) SB-Ge-NWT, and (c) SB-CS-NWT

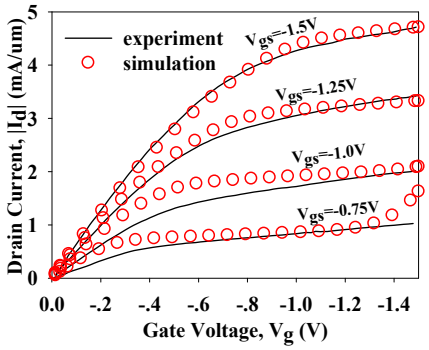

*Fig.*2 Agreement between simulation and experimental results [4] with calibrated parameters

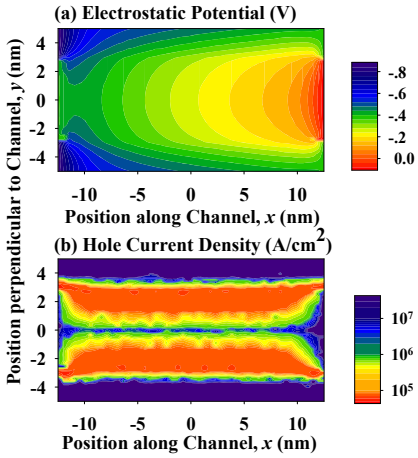

*Fig.*3 (a) Electrostatic potential and (b) hole current density of the cross section along SB-CS-NWT's channel.

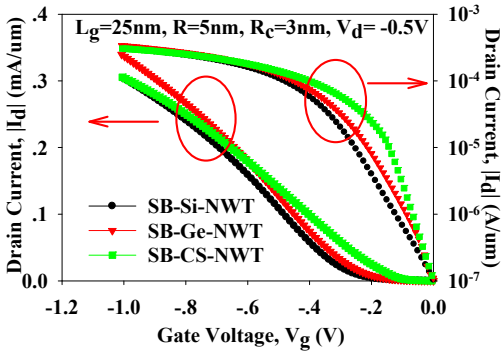

*Fig.*4 Transfer curves of SB-Si-NWT, SB-Ge-NWT, and SB-CS-NWT. L_g is 25nm, R is 5nm, R_c is 3nm, and V_d is -0.5V.

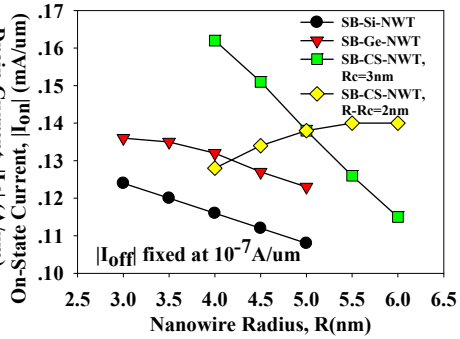

*Fig.*5 Normalized I_{on} versus R in different structures. R_c of SB-CS-NWT is either fixed at 3nm or varied with R. L_g is 25nm.

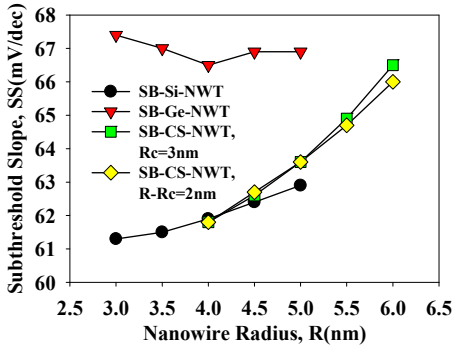

*Fig.*6 Sub-threshold slope versus R in different structures. R_c of SB-CS-NWT is either fixed at 3nm or varied with R. L_g is 25nm.

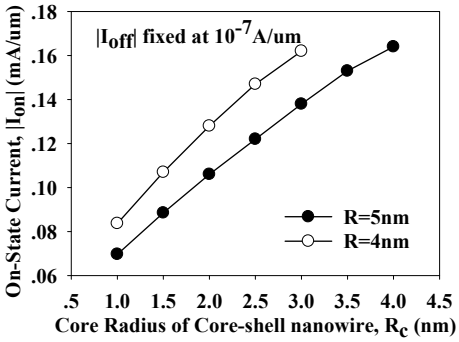

*Fig.*7 Normalized I_{on} versus R_c in different structures with R=4nm or R=5nm. L_g is 25nm.

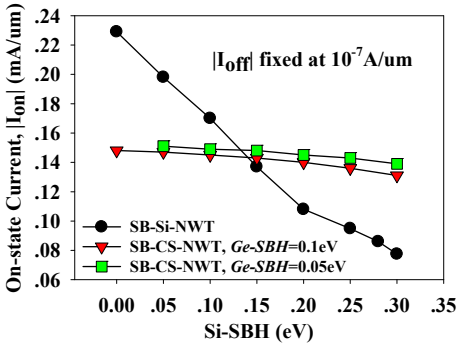

*Fig.*8 Normalized I_{on} versus *Si-SBH* for SB-Si-NWT and SB-CS-NWT. L_g is 25nm, R is 5nm, and R_c is 3nm.

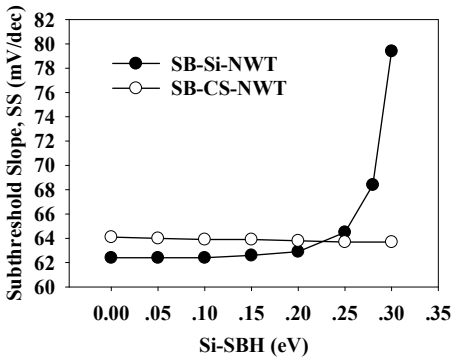

*Fig.*9 Sub-threshold slope versus *Si-SBH* for SB-Si-NWT and SB-CS-NWT. L_g is 25nm, R is 5nm, and R_c is 3nm.

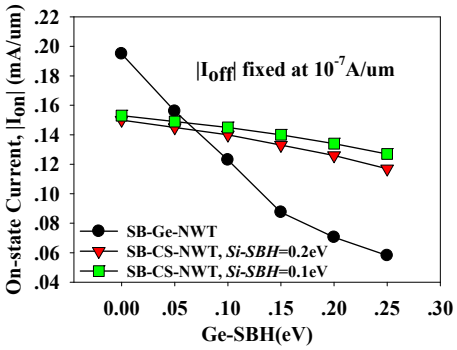

*Fig.*10 Normalized I_{on} versus *Ge-SBH* for SB-Ge-NWT and SB-CS-NWT. L_g is 25nm, R is 5nm, and R_c is 3nm.

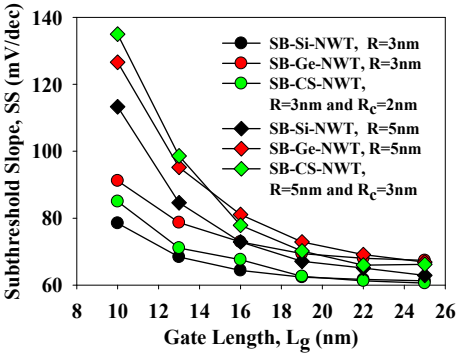

*Fig.*11 Sub-threshold slope versus L_g for different structures with R varied from 3 to 5nm and R_c varied from 2 to 3nm.