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Simple Fabrication Technique for an Array of Field-effect Transistors Using High-quality as-grown Single-walled Carbon Nanotubes from Dip-coated Catalyst by Substrate Surface Modification

Shinya Aikawa[1,2], Rong Xiang[1], Erik Einarsson[1], Shohei Chiashi[1], Junichiro Shiomi[1], Eiichi Nishikawa[2] and Shigeo Maruyama[1]

[1]Department of Mechanical Engineering, The University of Tokyo
7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan
Phone: +81-3-5841-6421 E-mail: maruyama@photon.t.u-tokyo.ac.jp
[2]Department of Electrical Engineering, Tokyo University of Science
1-3 Kagurazaka, Shinjuku-ku, Tokyo 162-8601, Japan

1. Introduction

A carbon nanotube field effect transistor (CNT-FET) has been investigated because of its potential applications in next-generation nanoscale organic devices. The electronic device particularly having a single-walled carbon nanotube (SWNT) as it gate channel exhibits excellent properties, with field-effect mobility as high as 10^5 cm^2 V^{-1} s^{-1} [1], high current capabilities of 10^9 A/cm^2 [2], a large I_{on}/I_{off} ratio of more than 10^6 [3] and quasi-ballistic transport in short channels [4]. However, in most previous reports post-processing such as drop-casting of dispersed SWNTs or deposition of electrodes was required after SWNT synthesis. Such fabrication processes may induce significant damage of the SWNTs, degrading the high-quality characteristics of as-grown SWNTs. Furthermore, the fabrication process using conventional MEMS techniques is quite challenging; it has many steps and limits catalyst coating to a dry process.

We previously reported that it is possible to pattern the growth of SWNTs using a liquid-based dip-coating by making hydrophilic and hydrophobic regions on a substrate surface [5]. The liquid process can realize batch fabrication for carbon nanotube electronic devices because of its scalability and cost-effectiveness. In our previous work, regions of a self-assembled monolayer (SAM) were selectively removed by vacuum ultraviolet or electron beam irradiation. Here we show CNT-FET having as-grown SWNTs from dip-coated catalyst could be simply fabricated using surface modification of substrate by SAM but without the removal process.

2. Experiment

P-type Si with 600 nm of oxide layer thickness was used as a substrate. The electrode array was firstly fabricated on the substrate using conventional photolithography and lift-off. Pd (15nm) and Au (50nm) were deposited using a vacuum evaporator and the thickness was monitored by a quartz oscillator system. Before surface modification by octadecyltrichlorosilane (OTS), the substrate with electrode array was subjected to an oxygen plasma treatment. To form the OTS-SAM on an OH-terminated SiO_2 surface, the substrate was submerged in a toluene-OTS solution (volumetric ratio of 500 and 1, respectively) for 15min and then withdrawn slowly. Using a similar liquid-based dip-coating process [6], the substrate was then dipped into a Co solution (0.01 wt% dissolved in ethanol) and was slowly withdrawn. The catalyst particles were calcined at 400 ^oC for 5min, followed by alcohol catalytic chemical vapor deposition (ACCVD) [7] at 800 ^oC for 10 min. The details of SWNT synthesis procedures have been described in previous reports [8-10].

After SWNT growth, the fabricated devices were characterized in ambient conditions by a semiconductor parameter analyzer (Agilent 4156C) using the substrate as a back-gate. To avoid damage due to electron beam and laser irradiation, scanning electron microscopy (SEM, Hitachi S-4800) observation and resonance Raman spectroscopy were performed after electrical property measurements.

3. Results and discussion

Figure 1 shows a SEM image of a fabricated device. By using liquid-based dip-coating, catalyst was deposited only along the electrode edge where the OTS-SAM could not be formed due to no presence of an OH-terminated surface [11]. Because an OTS surface is very hydrophobic, the site-selective growth of SWNTs could be obtained in the

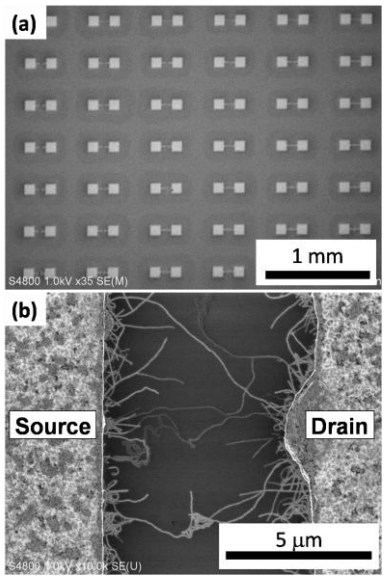

Fig.1 Typical SEM image of an array of SWNT-FETs (a) and nanotube channel between source/drain electrodes (b).

region. Figure 2 shows the transfer characteristics of a fabricated device operated at room temperature. The device has p-type unipolar characteristics that holes are the majority carrier, and has a threshold voltage (V_{th}) to suppress hole conductivity near $V_{GS} = 0$. The on-state ($V_{GS} < 0$) and off-state ($V_{GS} > 0$) region is clearly seen in the range of 6 orders of magnitude. However, some of the V_{th} are different from Fig. 2, possibly due to charge trapping by adsorbed molecules, mainly oxygen [12]. The value of V_{th} is sometimes negative and sometimes positive. Since the surface of a nanotube is sensitive to the ambient conditions, the value is roughly constant in air.

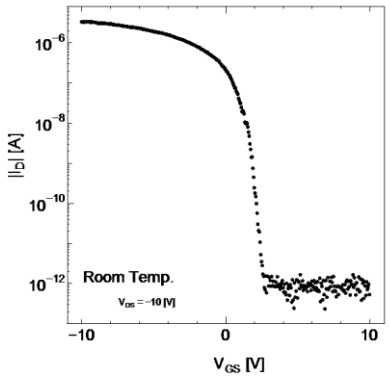

Fig.2 Transfer characteristics of the fabricated device with electrode width of 40 μm operated at room temperature. V_{DS} = -10 V.

Figure 3 illustrates the distribution of I_{on}/I_{off} ratios of the devices. The channel width of the fabricated device is 20 μm or 40 μm, while the gate length, set by the gap between the source/drain electrodes, is fixed at 5 μm. As shown the inset of Fig. 3, the yield of the fabricated structure with electrode widths of 20 μm and 40 μm achieved as high as 58% and 98%, respectively, among 60 measured devices. However, the lower I_{on}/I_{off} ratio increases when the wider electrode was used. This may be attributed to the presence of metallic tubes, as the probability of contact between SWNTs and electrodes increases. To analyze the fabricated

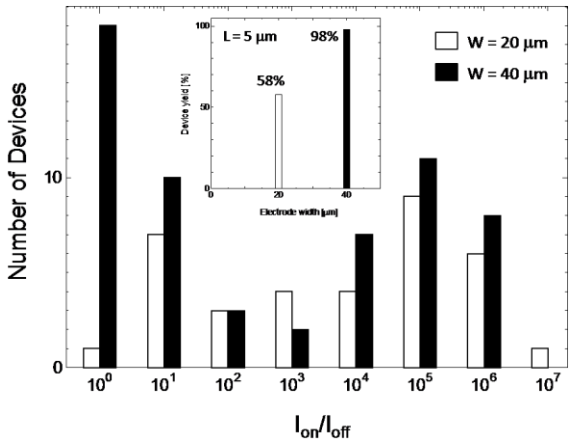

Fig.3 Histogram of I_{on}/I_{off} ratio of the fabricated devices. The open and solid bar means electrode width of 20 μm and 40 μm, respectively. The inset shows the device yield when channel length is 5 μm.

devices acting as functional FETs, which means drain current (I_D) depends on gate voltage (V_{GS}), we exclude those with I_{on}/I_{off} ratio of less than 100. Consequently, resultant functional FETs attained 45% (W = 20 μm) and 51.7% (W = 40 μm) yield for each structure. This yield is much better than previous reports by other groups [13,14].

4. Conclusion

An array of CNT-FETs employing as-grown SWNTs as the gate channel can be easily fabricated using hydrophobic surface functionalized by SAM and a liquid-based dip-coat process. FETs with a semiconducting SWNT bridge between the source/drain electrodes demonstrated high-quality characteristics, but the primary disadvantage of using as-grown SWNTs is the presence of metallic tubes. However, we believe that high yield fabrication of functional CNT-FETs may be possible by optimizing the gate channel length and width of contact electrodes.

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