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Epitaxial Graphene Field Effect Transistors on SiC substrate with Polymer Gate Dielectric

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1. Introduction

Recently, graphene has attracted much attention due to their high carrier mobility, 2D structure and a simple fabrication process compatible with standard CMOS technology. [1] To develop the graphene devices, however, numerous problems need to be overcome. Among them is the formation of gate dielectric. This is because the chemically inert nature of the graphene surface inhibits the deposition of uniform gate dielectric films. Plasma enhanced chemical vapor deposition (PECVD), commonly used in Si technology, can easily damage the graphene surface by the oxygen plasma. [2] Atomic layer deposition (ALD) method has advantages in thickness control and composition uniformity, but the high-k materials, mostly used in ALD such as HfO_2, show high density of defects in the dielectric layer. In this respect, polymer materials by spin coating method have advantages in low cost, easy fabrication and excellent dielectric properties. [3]

In this paper, the dielectric properties of polymer material (ZEP520a) were evaluated. ZEP520a, as a photoresist, shows better sensitivity and etch resistance as compared with PMMA, and thus has been widely used for device fabrications. Using the polymer, we fabricated graphene field effect transistors (FETs) on SiC substrate and demonstrated their electrical characteristics.

2. Experimental

A semi-insulating 6H SiC wafer (Si-terminated) was utilized as the starting substrate. The surface of the SiC wafer was cleaned in sulfuric peroxide mixture (H_2SO_4:H_2O_2=1:1) solution for 10 min, and the chemical oxide was etched in a diluted HF (H_2O:HF=30:1) solution for 1 min. The graphene layer was formed on the surface by annealing the substrate at 1600°C for 15 min. The graphene channel was then patterned by O_2 plasma etching. After pattering the graphene channel, a pair of Ti/Au (20 nm/50 nm) electrodes (source and drain) was deposited on the graphene layer by electron beam evaporation. The gate insulator was a 250 nm thick ZEP520a layer coated by spin coating method. The glass transition temperature (T_G) of ZEP520a is 105°C, the coated film was baked at 100, 110 and 120°C to investigate the impacts of the baking temperature on the dielectric characteristics of ZEP520a. To evaluate the dielectric properties of ZEP520a, Metal-Insulator-Si (MIS) capacitors were fabricated. Finally, a 150 nm thick Al was evaporated and the gate electrode was defined by photo lithography. Fig. 1 shows the optical microscope image of the graphene FETs on SiC substrate thus formed. The electrical characteristics of graphene FET were measured by B1500A semiconductor parameter analyzer.

3. Result and Discussion

Fig. 2 shows the leakage current characteristics of the MIS capacitors for various baking temperatures. As the baking temperature increases, the leakage current increases and the break-down voltage decreases. Also, a negative flat band voltage (V_{FB}) shift is observed as the baking temperature increases. It is understood that, at higher baking temperatures ($T>T_G$), more chemical bonds are broken in the dielectric layer, and fixed positive charges are generated. [4] For gate dielectric applications, therefore, the baking temperature of the polymer material should be lower than T_G. The C-V curve of the MIS capacitors, on the other hand, exhibits negligible hysteresis and memory windows for all the baking temperatures. This result implies absence of significant charge trapping/detrapping in the ZEP520a layer, and proves its potential as a good insulator for graphene FET. The dielectric properties of ZEP520a layer are summarized in table I.

Fig. 3 shows the Raman spectra of the SiC substrate before and after the graphitization annealing. After the annealing, three peaks related to graphene are prominent: the in-plane vibrational G peak (1590 cm^{-1}), the two-phonon G' peak (2730 cm^{-1}), and defect-induced D peak (1365 cm^{-1}). The inset in Fig. 2 is a typical low-energy electron diffraction (LEED) pattern from the graphene layer on the SiC substrate. A pronounced set of spots of the (1×1) graphene lattice is clearly shown. X-ray photoelectron spectroscopy (XPS) analysis (data not shown) also confirms formation of 2-3 monolayers of graphene.

Fig. 4 (a) and (b) shows the I_d–V_g and the I_d–V_d characteristics of the graphene FET with the ZEP520a gate dielectric (annealed at 100°C). The former indicates that the graphene device essentially exhibits the ambipolar conduction behavior, similar to that for FET based on exfoliated graphene. A large (~6V) negative Dirac voltage (V_{dirac}) shift was however observed in the present FET. The field effect mobility for this device is 580 cm^2/Vs for electrons, which is lower than those reported by other groups using epitaxial graphene (600 to 1200 [5] and 900 to 1520 [6] cm^2/Vs). We consider this degradation, as evidenced by the large V_{dirac} shift and the lower carrier mobility, to be due to insufficient optimization of the formation process of the polymer gate dielectric, whose betterment is under progress.

4. Conclusions

In summary, we fabricated graphene FETs with a polymer gate dielectric on SiC substrate, and investigated their electrical characteristics. Dielectric properties of the ZEP520a formed at and above T_G were degraded with shift in V_{FB} and low breakdown voltage. The graphene FET with the polymer gate dielectric shows negative V_{dirac} shift and low carrier mobility. Despite these non-ideal characteristics, however, we believe that the present results are enough to show the potential of the polymer dielectric (ZEP520a) as an effective insulating layer for graphene FETs. Further enhancement of the electrical characteristics is expected through optimization of the formation process of the polymer gate dielectric.

Acknowledgements

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References

[1] A. K. Geim and K. S. Novoselov, Nature Materials, vol.6, no.3, (2007), 183.

[2] Xuekun Lu et al., Applied Physic Letters, vol. 75, no. 2, (1999), 193

[3] J. Puigdollers et al., Organic Electronics, 5, (2004), 67.

[4] Moonkyung Na and Shi-Woo Rhee, Organic Electronics, 7, (2006), 205.

[5] Jakub Kedzierski et al., IEEE Trans. Electron Devices, vol. 55, No. 8, (2008), 2078.

[6] Y. M. Lin et al., Science, vol. 327, no. 5966 (2010), 662

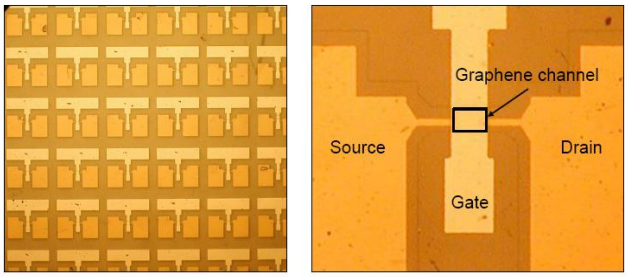


Fig. 1 Optical microscope image of graphene FET arrays.

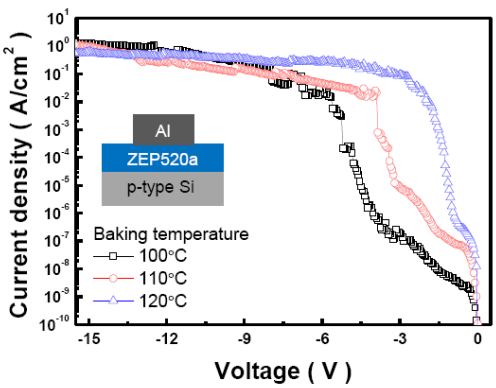


Fig. 2 I-V characteristics of MIS capacitors for three baking temperatures employed in the polymer fabrication process.

Table I Dielectric properties of ZEP520a layers with various baking temperature.

Bake Tem. (°C)	100	110	120
V_{FB} (V)	0.75	0.71	0.58
Memory Window (V)	0.016	0.055	0.093
Dielectric constant	1.6	1.7	2.0

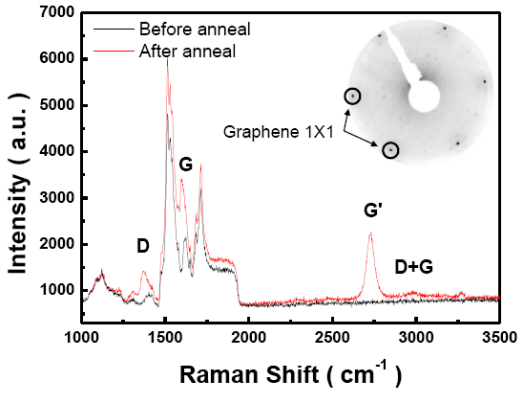
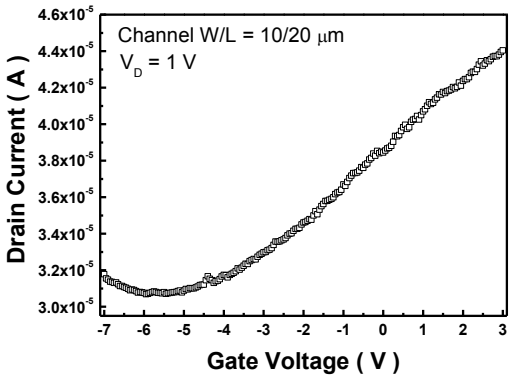
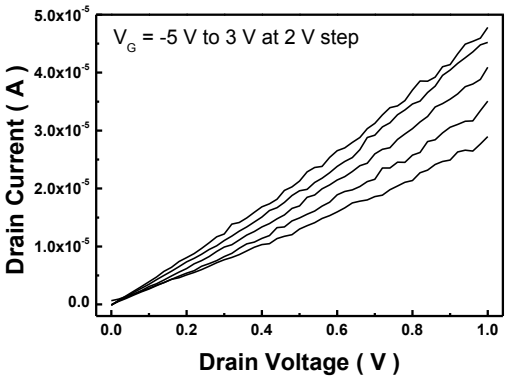


Fig. 3 Raman spectra of the SiC substrate before and after the graphitization anneal. Inset is a LEED pattern of the annealed 6H SiC substrate, indicating formation of epitaxial graphene.



(a)



(b)

Fig. 4 Electrical characteristics of the epitaxial graphene FET using the polymer gate dielectric. (a)I_d-V_g characteristics, (b) I_d-V_d characteristics.