A New Design Window of Fully Depleted Si Nanowire FETs

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Abstract – New design plane for multiple-gate MOSFETs beyond 25 nm technology node is presented. The proposed model is based on 3D simulation and physical analysis. Our results suggest that design optimization associated with the film dimension could be achieved for the multiple-gate MOSFETs. The nanowire FETs provide a more flexible design window, a common channel, and channel doping devices, due to an opposite trend of oxide thickness versus nanowire diameter when meeting the subthreshold swing limit.

I. Introduction

The International Technology Roadmap for Semiconductor (ITRS) has defined certain requirements along the roadmap, such as VDS, Ion, Lmin, etc., leading to emerging technologies, such as fully depleted silicon-on-insulator (FDSOI), multiple-gate (MG), and nanowire SOI MOSFETs [1]-[8]. The device scaling strategy has put much of attention on short-channel effect (SCEs) and subthreshold swing (SS). Because the conventional bulk MOSFETs usually require ultra-shallow junctions and precise channel doping profiles for controlling SCEs and leakage currents, eventually the doping scheme may become impractical due to random doping fluctuation [9]. Among emerging nanowire transistors, which can be done with an undoped body, have drawn much attention for good scaling capability and technology compatibility [10]-[11].

Fig. 1 shows the conventional CMOS design consideration [12]. Reduced channel depletion width (Wdm) improves the SCEs and thinner gate oxide thickness (t ox) increases the drive current. Though the technology scaling of each MOS device has been focused on its applicability to emerging devices is not yet clear. For example, instead of doping-controlled channel depletion width, SCEs can be controlled by using a thin silicon body in the PMOS SOI structure. Drain-induced barrier lowering (DIBL) can be suppressed by using a thin silicon body in the SiGe FinFET in nanometer regime [14]. The role of oxide thickness is another important factor in device scaling in addition to the bulk-soil gate technology. Monolithic gate delay (D) as well as DIBL and SS is lower determines the design window. Whichever of the DIBL and SS is lower determines the design window, defined by the shaded region on the bottom plan. On the other hand, we should also note the mobility degradation at high field subject to small diameter [11], [19]-[20]. Nanowire transistors suffer less degradation than the FinFET transistors do.

II. Design Consideration for Bulk MOSFETs

In our study of design window for emerging devices in the sub-25nm regime, we first reviewed conventional MOSFET structure. Fermi-Dirac statistics and drift-diffusion transport with modified local density approximation for carrier confinement were included in our device model. Both bulk MOSFETs and FinFETs have similar design windows due to their structure and electrical characteristics. The design consideration for bulk MOSFETs with different values of Wdm is shown in Fig. 2. Higher doping (or thinner Wdm) results in a smaller DIBL. Designers have to consider the SCE parameter as in Fig. 1. Therefore, the design tradeoff among various factors such as SCEs, SS, and critical oxide-field of gate leakage can be made within the design window of dimensional parameters. Wdm impact of bulk MOSFET complicates doping profile for SCEs control whereas the channel thickness of multiple gate MOSFET has a similar effect but at a far different extent. Fig. 3 shows the analysis for conventional bulk MOSFETs. A good choice of Lmin/mWdm is 2, considering SCEs [12]. In conventional structure, the gate oxide capacitance Cg and channel capacitance Cc are in series, later of which reflects the capacitance of the inversion charge. The body-effect coefficient (m), implying SS, is simply a combination which reflects the capacitance of the inversion charge. The dimension of FinFET fin width (Wfi) and nanowire diameter (D) is set to half channel length. In our study, the nominal case has Wsi = 4Wdm and D = 5 nm, metallurgical channel length (L) of 10 nm, gate oxide of 0.6 μm, buried oxide of 200 nm, and fin height/width (Hsi/Wsi) of 10/1. Fig. 4 shows the simulated Lmin vs. Vth in Fig. 6 shows the simulated Ion/Ion vs. Vth characteristics for FinFET and nanowire transistors with same Wsi and D. Lots of the cases are comparable via gate work function adjustment for fair comparison. The DIBL and SS data are shown in Fig. 13 for various FinFET transistors. Fig. 8 shows the C-V characteristics for FinFET transistors with different Wsi. To assess the speed performance for logic application in Wsi scaling, conventional CV/Ion metric is evaluated, as shown in Fig. 9. Fig. 10 shows DIBL and SS versus Wsi for FinFETs. The nanowire structure of nanowire has very good gate controllability. Fig. 11 shows C-V characteristics for nanowire transistors with different D’s. All nanowire cases are already biased into strong inversion regime at high VGS. Fig. 12 shows the performance projection in D scalability based on Wsi/Drain. The performance is sensitive to D, shown in Fig. 13, as compared with that of FinFETs.

IV. New Design Window of Fully Depleted Nanowire

According to our results, when Wsi (or D) decreases, the electrical characteristics of MG-FinFET and nanowire transistors suffer less degradation than the FinFET transistors do.

V. Conclusion

New design methodology for MG MOSFETs beyond 25 nm technology node is proposed. The tradeoff among the dimensional dependent physical insight into device design criterion, Fig. 14 shows the diagram of nanowire transistor capacitances network in which electron charge density increases with diameter. The design plane is shown in Fig. 17 for a high field subject to small diameter.

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References
Fig. 1 \( t_{ox} \) versus \( W_{dm} \) design plane for conventional bulk MOSFETs.

Fig. 2 Predicted conventional MOSFET design plane.

Fig. 3 Conventional MOSFET design factors.

Fig. 4 3-D view of the FinFET transistor device where \( y \) axis in the direction along the channel and \( x-z \) surface corresponds to the cross section of the wire (not to scale).

Fig. 5 3-D view of Nanowire transistor device where \( y \) axis in the direction along the channel and \( x-z \) surface corresponds to the cross section of the wire (not to scale).

Fig. 6 \( I_{DS} \) versus \( V_{GS} \) characteristics for FinFET and nanowire transistors with same channel dimension \((W_s/D)\) of 5 nm.

Fig. 7 DIBL and SS versus \( W_s \) for various FinFET transistors.

Fig. 8 Gate capacitance versus \( V_{GS} \) for FinFET transistors with different \( W_s \)’s.

Fig. 9 CV/I\(_{on} \) versus \( W_s \) for various FinFET transistors.

Fig. 10 DIBL and SS versus diameter for various nanowire transistors.

Fig. 11 Gate capacitance versus \( V_{GS} \) for nanowire transistors with different D’s.

Fig. 12 CV/I\(_{on} \) versus diameter for various nanowire transistors.

Fig. 13 CV/I\(_{on} \) versus fin width for various FinFET and nanowire transistors.

Fig. 14 Multiple-gate FD SOI MOSFETs design factors.

Fig. 15 Multiple-gate FD SOI MOSFETs design window under acceptable SS (120 mV/dec) and DIBL (160 mV/V) limits.

Fig. 16 Schematic diagram of the nanowire transistor capacitances network [19].

Fig. 17 3D representation of MG FD SOI design window.