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A New Design Window of Fully Depleted Si Nanowire FETs

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Abstract – New design plane for multiple-gate MOSFETs beyond 25 nm technology node is presented using numerical 3D simulation and physical analysis. Our results suggest that design optimization associated with the film dimension could be achieved for the multiple-gate MOSFETs. The nanowire FETs provide a more flexible design window, a compared with conventional bulk devices, due to an opposite trend of oxide thickness versus nanowire diameter when meeting the subthreshold swing limit.

I. Introduction

The International Technology Roadmap for Semiconductor (ITRS) has defined certain requirements along the scaling roadmap, such as V_{DD}, I_{on}, I_{off}, etc., leading to emerging technologies, such as fully depleted silicon-on-insulator (FDSOI), multiple-gate (MG), and nanowire SOI MOSFETs [1]-[8]. The device scaling strategy has put much of attention on short-channel effect (SCEs) and subthreshold swing (SS). Because the conventional bulk MOSFETs usually require ultra-shallow junctions and precise channel doping profiles for controlling SCEs and leakage currents, eventually the doping scheme may become impractical due to random doping fluctuation [9]. Among emerging devices, MG and nanowire transistors, which could be done with an undoped body, have drawn much attention for good scaling capability and technology compatibility [10]-[11].

Fig. 1 shows the conventional CMOS design consideration [12]. Reduced channel depletion width (W_{dm}) improves the SCEs and thinner gate oxide thickness (t_{ox}) increases the drive current. Though the conventional CMOS design window has been studied, its applicability to emerging devices is not yet clear. For example, instead of doping-controlled channel depletion width, SCEs can be controlled by a thin fin silicon body in the PMOS FinFET [13]. Drain-induced barrier lowing (DIBL) can be suppressed by using a thin fin silicon body in the SiGe FinFET in nanometer regime [14]. The role of oxide thickness is another important factor in device scaling in addition to "high-k metal gate" and channel doping [15]. Previous works have provided device design methodologies, but the complete design window requires further study. In this work, we present design methodologies for FinFETs and nanowire MOSFETs when pursuing optimal performance and come up a new design window using the 3D TCAD simulations.

II. Design Consideration for Bulk MOSFETs

In our study of design window for emerging devices in the sub-25nm regime, we first reviewed conventional MOSFET structure. Fermi-Dirac statistics and drift-diffusion transport with modified local density approximation for carrier confinement were included in simulation [16]. The simulated DIBL vs. channel doping for bulk MOSFETs with same t_{ox}, implying W_{dm} dependence as W_{dm} is set by doping (Fig. 2). Higher doping (or thinner W_{dm}) shows lower DIBL, which allows thicker t_{ox}, as illustrated by the SCE boundary in Fig. 1. For another design consideration of subthreshold swing (SS) at fixed t_{ox}, higher SS is predicted for reduced W_{dm} when channel doping increases.

Design tradeoff among various factors such as SCEs, SS, and critical oxide-field of gate leakage can be made within the design window of dimensional parameters. W_{dm} impact of bulk MOSFET complicates doping profile for SCEs control whereas the channel thickness of multiple gate MOSFET has a similar effect but at a far different extent. Fig. 3 shows the analysis for conventional bulk MOSFETs. A good choice of L_{min}/mW_{dm} is 2, considering SCEs [12]. In conventional structure, the gate oxide capacitance C_{ox} and channel capacitance C_{si} are in series, later of which reflects the capacitance of the inversion charge. The body-effect coefficient (m), implying SS, is simply a combination of C_{ox} and C_{si}. Substituting m of (2) into (1) yields (4) in Fig. 3. If we assume the $3t_{ox}$ term of (4) is relatively small, it is found $W_{dm} \approx$ 1/2*L for acceptable SCEs and SS in conventional bulk design.

III. Design Consideration for Advanced Structure

Following the same methodology for bulk MOSFETs, we investigate the design window for nanowire transistors. The FinFET and nanowire nMOSFET structures used in 3D TCAD simulation are shown in Fig. 4 and Fig. 5, respectively. In order to effectively suppress doping fluctuation, the undoped body in dimension of FinFET fin width (W_{si}) [9] and nanowire diameter (D) is set to half channel length. In our study, the nominal case has W_{si} and D of 5 nm, metallurgical channel length (L) of 10 nm, gate oxide of 0.6 nm, buried oxide of 200 nm, and fin height/width (H_{si}/W_{si}) ratio of 4 [10], following the ITRS roadmap [17].

Fig. 6 shows the simulated I_{DS} vs. V_{GS} characteristics for FinFET and nanowire transistors with same W_{si} and D. I_{off}'s of all cases are comparable via gate work function adjustment for fair comparison. Fig. 7 shows the predicted DIBL and SS versus W_{si} for various FinFET transistors. Fig. 8 shows the C-V characteristics for FinFET transistors with different W_{si}'s. To assess the speed performance for logic application in W_{si} scaling, conventional CV/I_{on} metric is evaluated, as shown in Fig. 9. Fig. 10 shows DIBL and SS versus D for various nanowire transistors. The surrounded gate structure of nanowire has very good gate controllability. Fig. 11 shows C-V characteristics for nanowire transistors with different D's. All nanowire cases are already biased into strong inversion regime at high V_{GS}. Fig. 12 shows the performance projection in D scaling based on CV/I_{on}. Its predicted performance is insensitive to D, shown in Fig. 13, as compared with that of FinFETs.

IV. New Design Window of Fully Depleted Nanowire

According to our results, when W_{si} (or D) decreases, the electrical characteristics of MG structure improve. To understand the physical insight into device design criterion, Fig. 14 shows the analysis for MG SOI MOSFETs based on the concept of fully depleted (FD) substrate. A good choice of L_{min}/mW_{dm} is 3/2 when accounting for DIBL in MG structure [14]. In the fully depleted structure [18], there are two oxide capacitances, C_{ox1} and C_{ox2}, and C_{si} on the cut plane of Fig. 4 and Fig. 5 in x direction. Using the same form as in bulk structure, the capacitive coupling factor is C_{dm}/C_{ox1}, but in fact C_{ox1} is the gate capacitance for the front gate and C_{dm} ($= C_{si}C_{ox2}/C_{si}+C_{ox2}$) is the serial capacitance between the inversion channel and the back-gate electrode. In common symmetrical gate structure, C_{ox1} is equal to C_{ox2}. We can derive $m \approx 1 + (3t_{ox}/(3t_{ox}+W_{dm}))$ by substituting $C_{ox1} = C_{ox2} = C_{ox} = \varepsilon_{ox}/t_{ox}$ and $C_{si} = \varepsilon_{si}/t_{si}$ into (2) of Fig. 14. Furthermore, SS is derived in (3). Substituting m of (2) into (1) then yields (4). Given that the ideal factor for *m* is 1, the optimal design of W_{dm} should fall into 2/3 * L, applicable to both FinFET and nanowire results in Fig. 9 and Fig. 12, respectively. As compared with the bulk case with a bounded design window, the nanowire transistor has a more flexible design window shown in Fig. 15, which is only limited to the lower DIBL curve in which SS is no longer a limiting factor. In contrast to classical bulk study, the capacitance of total C_{si} increases as the nanowire diameter increases and hence the SS curve in Fig. 15 shows an opposite trend to that in Fig. 1. Such similar phenomenon was also shown in quantum capacitance limit [19]. Fig. 16 shows the diagram of nanowire transistor capacitances network in which electron charge density increases with diameter.

Fig. 17 shows a 3D representation for MG FD SOI design window. Whichever of the DIBL and SS is lower determines the design plan, defined by the shadowed region on the bottom plan. On the other hand, we should also note the mobility degradation at high field subject to small diameter [11], [19]-[20]. Nanowire transistors suffer less degradation than the FinFET transistors do.

V. Conclusion

New design methodology for MG MOSFETs beyond 25 nm technology node is presented. The fin/wire dimension dependent performance is investigated. Due to the opposite trend of gate oxide thickness versus nanowire diameter at given SS limit, nanowire FETs provide a more flexible design window.

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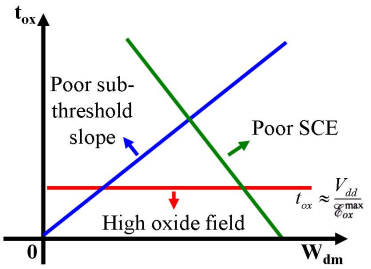

Fig. 1 t_{ox} versus W_{dm} design plane for conventional bulk MOSFETs.

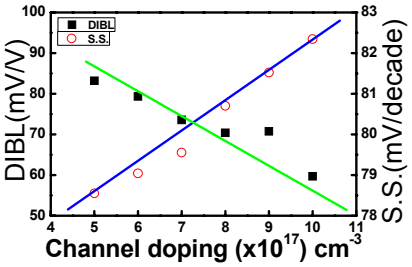

Fig. 2 Predicted conventional MOSFET design plane.

(1) Bulk SCEs	$\frac{L_{min}}{mW_{dm}} \approx 2$
(2) Bulk body-effect coefficient	$m \equiv 1+\frac{C_{dm}}{C_{ox}} = 1+\frac{3t_{ox}}{W_{dm}}$
(3) Bulk Subthreshold Swing	$SS = \frac{kT}{q}\ln(10)(1+\frac{C_{dm}}{C_{ox}})$
(4) Bulk Max Depletion Width	$W_{dm} \approx \frac{L_{min}}{2} - 3t_{ox}$

Fig. 3 Conventional MOSFET design factors.

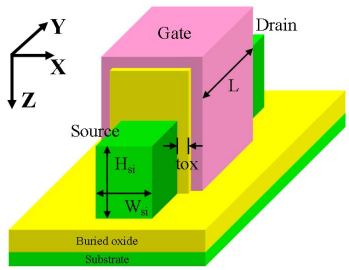

Fig. 4 3-D view of the FinFET transistor device where y axis in the direction along the channel and x-z surface corresponds to the cross section of the wire (not to scale).

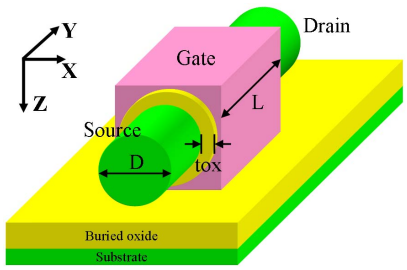

Fig. 5 3-D view of Nanowire transistor device where y axis in the direction along the channel and x-z surface corresponds to the cross section of the wire (not to scale).

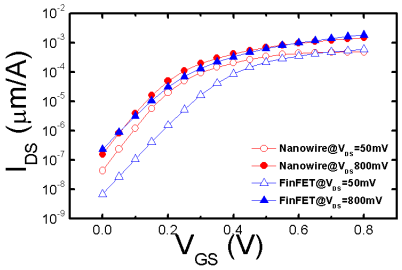

Fig. 6 I_{DS} versus V_{GS} characteristics for FinFET and nanowire transistors with same channel dimension (W_{si}/D) of 5 nm.

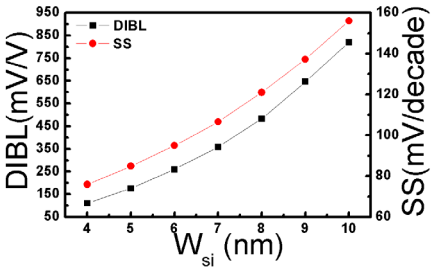

Fig. 7 DIBL and SS versus W_{si} for various FinFET transistors.

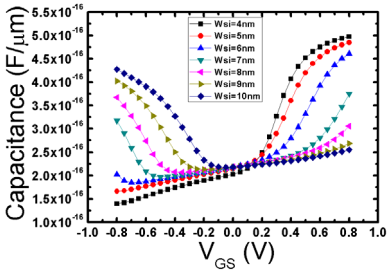

Fig. 8 Gate capacitance versus V_{GS} for FinFET transistors with different W_{si}'s.

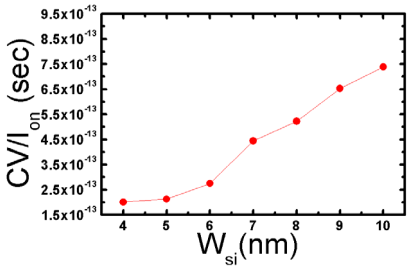

Fig. 9 CV/I_{on} versus W_{si} for various FinFET transistors.

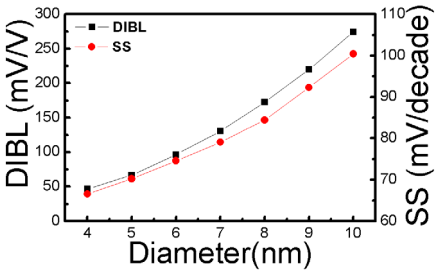

Fig. 10 DIBL and SS versus diameter for various nanowire transistors.

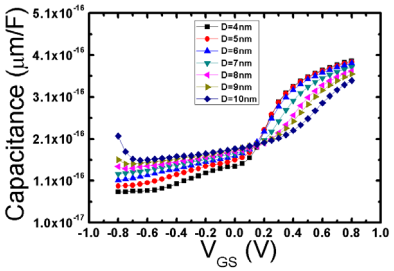

Fig. 11 Gate capacitance versus V_{GS} for nanowire transistors with different D's.

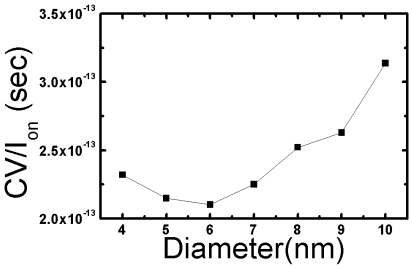

Fig. 12 CV/I_{on} versus diameter for various nanowire transistors.

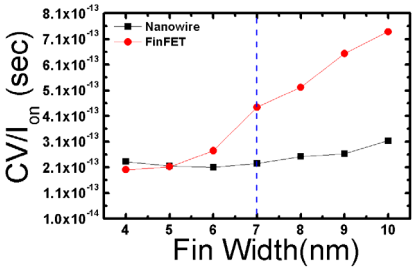

Fig. 13 CV/I_{on} versus fin width for various FinFET and nanowire transistors.

(1) SOI SCEs	$\frac{L_{min}}{mW_{dm}} \approx \frac{3}{2}$
(2) SOI body-effect coefficient	$m \equiv 1+\frac{C_{dm}}{C_{dm}+C_{ox}} = \frac{W_{dm}+6t_{ox}}{W_{dm}+3t_{ox}}$
(3) SOI Subthreshold Swing	$SS = \frac{kT}{q}\ln(10)(1+\frac{C_{dm}}{C_{dm}+C_{ox}})$
(4) SOI Fin Width (= W_{dm})	$W_{dm} \approx \frac{2}{3}L_{min}(\frac{W_{dm}+3t_{ox}}{W_{dm}+6t_{ox}})$

Fig. 14 Multiple-gate FD SOI MOSFETs design factors.

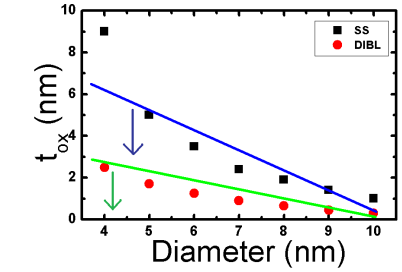

Fig. 15 Multiple-gate FD SOI MOSFETs design window under acceptable SS (120 mV/dec) and DIBL (160 mV/V) limits.

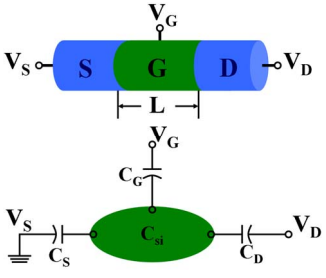

Fig. 16 Schematic diagram of the nanowire transistor capacitances network [19].

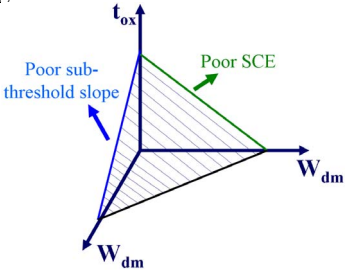

Fig. 17 3D representation of MG FD SOI design window.