

Lateral High-Voltage 4H-SiC MOSFETs

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1. Introduction

Silicon carbide is a promising semiconductor for high-temperature, high-power, and high-frequency applications because of its wide band gap, high breakdown field, and high saturation velocity. In recent years, the reduced surface field (RESURF) structure has been widely used in lateral SiC power device due to the good trade-off relationship between breakdown voltage and on-resistance [1]. In this paper, we report the characteristics of lateral high-voltage 4H-SiC MOSFETs built on the Si-face of a 4H-SiC semi-insulating substrate. The drain induced barrier lowering (DIBL) effect in these devices is also investigated. DIBL is not as significant as in the conventional n-MOSFET with the same channel length because most of the voltage drop is supported by RESURF region and the lateral depletion in the body is reduced.

2. Device Structure and Experiment Result

Device Structure

The proposed power MOSFET, as shown in figure 1, was fabricated on a p-type epilayer on a 4H-SiC semi-insulating wafer. The composition of the epilayer is $0.1\mu\text{m}/1\times10^{16}\text{cm}^{-3}$ and $2\mu\text{m}/5\times10^{16}\text{cm}^{-3}$, beginning from the top. The doping concentration near the surface was intentionally reduced to ensure good channel mobility due to less impurity scattering. The total dose in the p-layer must not exceed $1.3\times10^{13}\text{ cm}^{-2}$ to ensure complete depletion in the drift region under high reverse bias [2]. Drift region was separated into two zones in order to reduce the on-resistance without lowering the breakdown voltage. Zone 1 and zone 2 were formed by implantation of nitrogen with doses of 8×10^{12} and $1.02\times10^{13}\text{ cm}^{-2}$ into p-type epilayer, respectively. Source and drain were made by implantation of phosphorous, and p+ region was made by implantation of aluminum, all at 650°C . Activation for all implant species was done at 1650°C for 30 minutes in argon. Graphite cap was used during implant activation to preserve good surface morphology. After RCA clean, gate oxidation was done at 1180°C for 6 hours in dry oxygen ambient, followed by NO annealing at 1175°C for 2 hours. The equivalent oxide thickness is about 900 angstrom from a CV measurement. Contact metal consisting of 20 nm Ti and 100 nm Ni was used in the n+ drain and source. A layer of 20 nm Ti, 120 nm Al, and 100 nm Ni was employed for P+ body contact. Then, a rapid thermal annealing was done at 1200°C for 3 minutes in vacuum to sinter these contact

metal at the same time. Al/Ti field plates were deposited and extended over the RESURF region from the drain edge by $13\ \mu\text{m}$ to suppress the surface field around the junction edges.

Experiment Results

Fig. 2 illustrates the on-state and reverse characteristic of a proposed device with $W = 200\ \mu\text{m}$, $L_{ch} = 5\ \mu\text{m}$, $L_d = 160\ \mu\text{m}$, $L_{fp,g} = 0\ \mu\text{m}$ and $L_{fp,d} = 13\ \mu\text{m}$. The device shows normally off characteristics with a threshold voltage of 2.9 V . The specific on-resistance extracted at $V_{gs} = 40\text{ V}$ and $V_{ds} = 0.1\text{ V}$ is found to be $1113\text{ m}\Omega\cdot\text{cm}^2$ and the breakdown voltage is 1400 V . Fig. 3 depicts the normalized on-resistance, channel resistance and drift resistance at different temperatures for the proposed devices. The channel resistance and the channel mobility are estimated from a test MOSFETs with $L_{ch} = 100\ \mu\text{m}$. The measured field effect mobility at room temperature is $35\text{ cm}^2/\text{Vs}$. The drift region resistance is measured from a four point probe structure which has the same sheet resistance as the drift region. As can be seen in Fig. 3, R_{on} and R_{drift} increase monotonically with temperature. On the other hand, the channel resistance is decreased with temperature because of increasing mobility. This indicates the contribution of R_{on} is mostly from the R_{drift} in these devices despite the poor channel mobility in SiC.

The I_d - V_g characteristics at different V_d for a device with $L_{ch} = 3\ \mu\text{m}$ and $L_d = 20\ \mu\text{m}$ are compared in Fig. 4. The threshold voltage is defined as the gate voltage at which the drain current reaches $1\ \mu\text{A}$. Fig. 5 shows the dependence of drain voltage on threshold voltage for high-voltage and standard low-voltage devices with 3, 5 and $100\ \mu\text{m}$ channel lengths. It is observed that V_t is significantly decreased with higher V_d for low-voltage devices, especially for channel length of 3 and $5\mu\text{m}$. The DIBL effect which is defined as dV_t/dV_d is significant because the p-body is lightly doped in these devices [3]. On the other hand, the HV devices, even with $L_{ch} = 3\ \mu\text{m}$, do not show DIBL effect because most of the voltage drop is supported by RESURF region. Therefore, the lateral extension of depletion in p-body region is not severe.

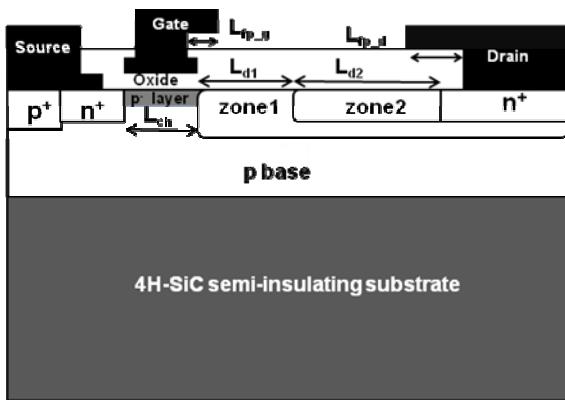


Fig. 1 Lateral 4H-SiC two-zone RESURF MOSFETs on a semi-insulating substrate

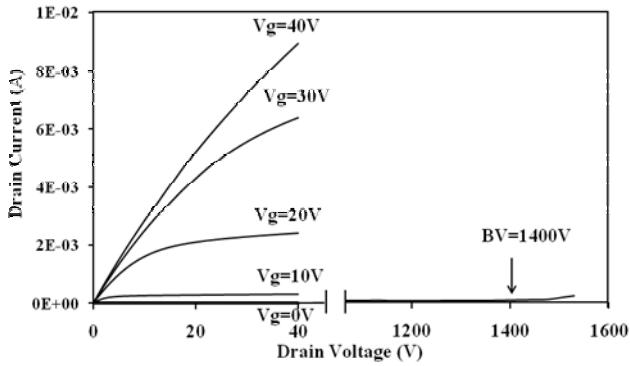
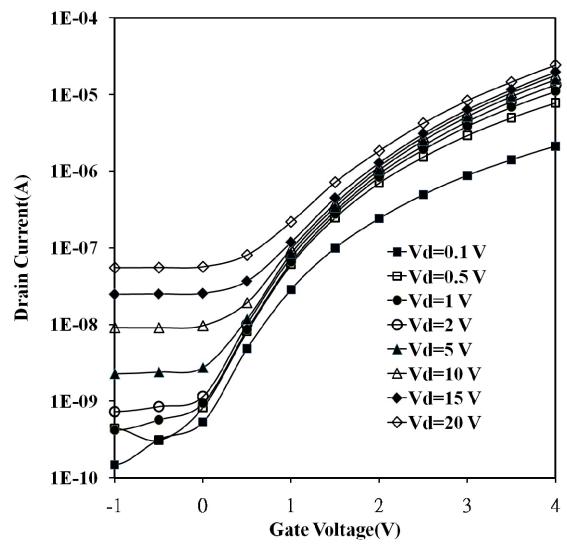


Fig. 2 On-state and reverse blocking characteristics of a device with $L_{ch} = 5 \mu\text{m}$, $L_{d1} = L_{d2} = 80 \mu\text{m}$

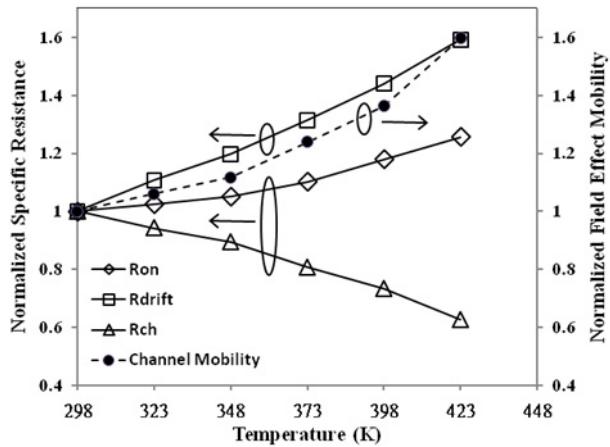


Fig. 3 Normalized resistances versus temperature in a device with $L_{ch} = 3 \mu\text{m}$ and $L_{drift} = 20 \mu\text{m}$, and normalized field effect mobility from a test device with $L_{ch} = 100 \mu\text{m}$.

Fig. 4 I_d - V_g curves of a device with $L_{d1} = L_{d2} = 10 \mu\text{m}$ and $L_{ch} = 3 \mu\text{m}$ at different V_d .

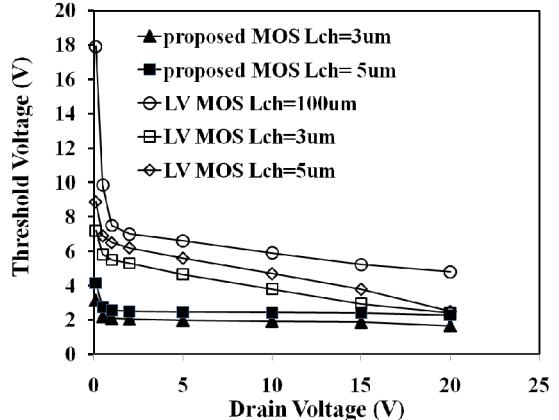


Fig. 5 Threshold voltages as a function of drain voltage for the proposed and LV devices with channel lengths of 3, 5 and 100 μm .

3. Conclusion

In summary, a lateral 1400V SiC MOSFET is fabricated. The field effect mobility is about $35 \text{ cm}^2/\text{Vs}$, extracted from a test MOSFET with $L_g = 100 \mu\text{m}$. Despite the lightly doped body, DIBL effect is not as significant as in low-voltage MOSFETs. More updated measurement results will be presented at the conference.

Acknowledgement

This work is supported by National Science Council of Taiwan, R. O. C. under Contract No. NSC98-2221-E-007- 118.

References

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