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Development of Versatile Backside Via Technology for 3D System on Chip

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1. Introduction

Demand for high-performance and highly integrated system has been significantly increasing in correspondence to future needs. To meet these requirements, three dimensional (3D) integration technology has attracted attention, because it vertically stacks multiple LSI chips into one stacked chip. In order to realize high performance and highly integrated systems, we proposed 3D super chip that stacks various kinds of functional blocks such as processor, memory, sensor, logic, analog, MEMS, and power ICs one stacked chip through high density through silicon vias (TSVs) and micro-bumps as shown in Fig. 1[1]. For the super chip, there are two process technologies to form high density TSV, which means “front side via” and “backside via” processes. However, the front side via process has challenges to form vias through multi-layers structure composing of thick inter layer dielectric (ILD) layers, poly-Si layers, and Si substrate. Recently, in high-end processor chips, they have 8-9 metal layers. Therefore, it is difficult to etch the different kinds and multi-layered materials. In order to solve this issue, we proposed the backside via formation process, which fabricate vias with high speed.

In this study, we developed several key technologies for the formation of fine pitch backside via. The fine pitch backside via of 10 μm diameter and 30 μm depth was successfully formed. To verify the backside via process technology, we fabricated the stacked test module. The electrical characteristics of the backside via were successfully evaluated.

2. Development of the backside via process

Fig. 2 shows the schematic process flow of the backside via we proposed. A fabricated LSI chip was precisely aligned and face-down bonded to supporting wafer such as glass or silicon by glue layer with high thermal stability. Then, the chip is uniformly thinned down to 30 μm by mechanical grinding and chemical mechanical polishing (CMP) process. A dielectric layer was deposited onto the backside of thinned chip as an isolation layer. We applied a thick SiO_2 layer of 1 μm, because it also used as a hard mask layer for the isolation contact etching. Photo resist was spin-coated and patterned for the deep via etching. The Si substrate was etched from the backside by time-modulation etching process without notching problem. Dielectric layer was etched until to expose a bottom metal layer. Thin SiO_2 dielectric layer was deposited into the deep via. SiO_2 layer on the bottom metal layer must be removed to electrically connect. However, it is very challenges to form the mask for the etching of SiO_2 layer into the high aspect-ratio and fine size via by normal PR photolithography process. Because PR would be remained even after developing, hence it induces the etching failure. In order to avoid this issue, we adopted thick SiO_2 hard mask. The oxide thickness on the backside of chip is thicker than the oxide thickness on the bottom metal layer. By using the difference of SiO_2 thickness, thin bottom SiO_2 layer was contact etched without the PR mask. Barrier layer of Ta and seed layer of Cu were s sequentially puttered into the backside via. After patterning the PR mask, the backside via was filled with Cu by electroplating method. Low viscosity PR and the controlled curing process were used do not enter into the via during the spin-coating process. Such PR patterning process is important to form the void-free Cu via. Then, Sn layer was deposited on the Cu via of the chip backside by evaporation method. After lift-off process, Cu/Sn micro-bumps were formed on the backside via. Seed layer and barrier layer was removed by etching processes, respectively. The supporting glass wafer was diced. Finally, the test chip bonded with glass chip was bonded to the substrate with non-conductive film (NCF) by thermo-compression bonding.

3. Evaluation of the test module with the backside via

We developed several key technologies such as the fine sized via etching, the isolation contact etching of the bottom area, and void-free Cu filling for the backside via formation. Normally, the notch phenomenon was happed by the accumulated positive ions on isolation surface during BOSCH etching process. For the fine size TSV formation, the notch issue becomes more severe. The notching phenomena cause the failures of post process such as formation of isolation layer and seed layer for the backside via formation. In this study, we adopted the time-modulation etching process to avoid the notching. Fig. 3 shows SEM cross-sectional images after the Si etching. TSV was formed through Si substrate with 30 μm thick and stopped on the isolation layer with 1 μm

thick. As clearly seen the figure, the notch is only 0.1~0.3 μm even after 30 % over etching of Si. After etching Si, the isolation layer of 1 μm thick was etched to expose the metal layer as shown in Fig. 4. We optimize Cu via filling process. The deep TSV of 10 μm in diameter and 30 μm depth was filled without void and well connected to the metal layer as shown in Fig. 5.

By applying these technologies, we fabricated the test module including daisy chain to evaluate the feasibility of 3D integration. Fig. 6 shows SEM cross-sectional image of the fabricated test module including the TEG circuits and the daisy chain. TSV of 10 μm in diameter and 30 μm depth is filled without voids and well connected to metal layer. We evaluate the electrical resistance of Cu TSV in the daisy chain as shown in Fig. 7. It shows the linear I-V characteristics. It means that the fine sized backside via was successfully implemented.

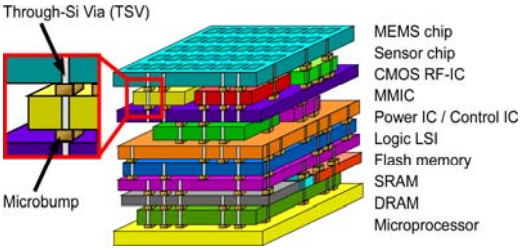

Fig. 1 Conceptual structure of 3D super chip.

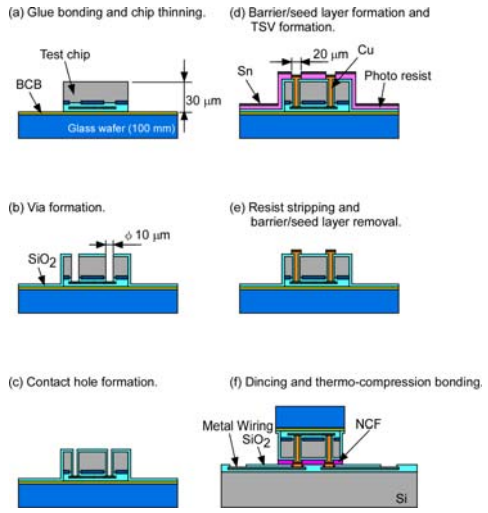

Fig. 2 Fabrication process using backside via process.

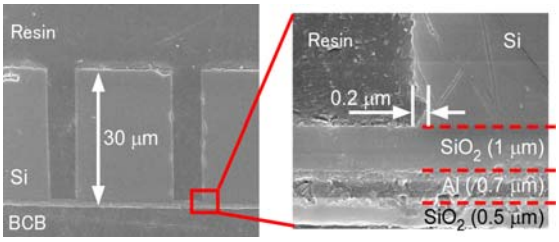

Fig. 3 Cross-sectional SEM image of after Si etching.

4. Conclusion

In this paper, we described the backside via technology for 3D integration. Fine Cu TSV of 10 μm in diameter and 30 μm depth was successfully formed from the backside of the thinned chip. The test chip with the backside via was bonded to Si substrate through Cu/Sn micro-bumps and NCF tape, and showed superior I-V characteristics. The backside via technology is so versatile that different kinds of chips can be easily stacked to fabricate the 3D system on chip.

References

[1] T. Fukushima and M. Koyanagi, *et al.*, *IEDM Tech. Dig.*, pp. 359-362 (2005).

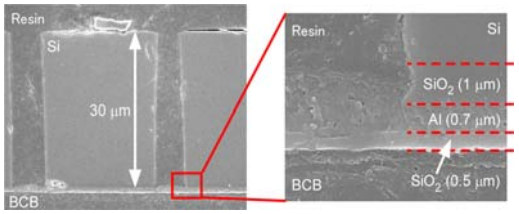

Fig. 4 Cross-sectional SEM image of after ILD etching.

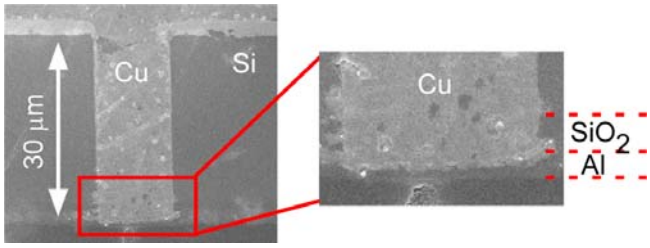

Fig. 5 Cross-sectional SEM image of electroplated Cu TSV.

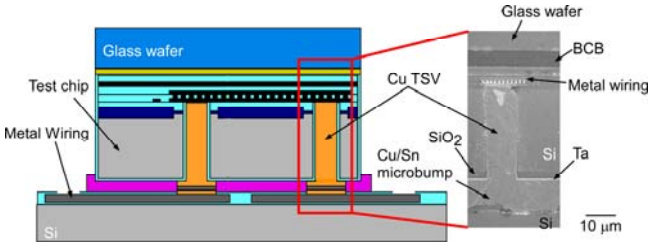

Fig. 6 Configuration cross-structure of the test chip and cross-sectional SEM image of Cu TSV.

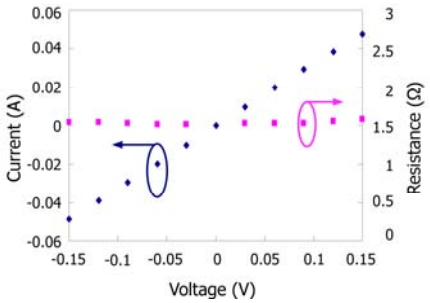

Fig. 7 I-V and R-V characteristics of Cu TSV of 10 μm in diameter and 30 μm depth.