Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp241-242

Stress Mapping of Silicon Surrounded by Various Through Silicon Via (TSV) Patterns using Polychromator-Based Multi-Wavelength Raman Spectroscopy

Alastair David Trigg[1], Li Hong Yu[1], Cheng Cheng Kuo[1], Rakesh Kumar[1], Dim Lee Kwong[1], Takeshi Ueda[2], Toshikazu Ishigaki[2], Kitaek Kang[2] and Woo Sik Yoo[2]

[1]Institute of Microelectronics/A*STAR, 11 Science Park Road, 117685, Singapore
[2]WaferMasters, Inc., 246 East Gish Road, San Jose, CA 95112, U.S.A.
Phone: +65-6770 5455 Fax: +65-6773 1914 E-mail: alastair@ime.a-star.edu.sg

1. Introduction

Traditional device scaling is facing increasing difficulties as it approaches its physical limits. Therefore, in parallel with driving dimensions ever smaller to follow Moore's law, there is increasing emphasis on using advanced packaging technologies to provide functional improvements with existing device dimensions, sometimes describes as "More than Moore". For many applications, the use of stacked, thinned chips to provide higher packing density has become commonplace. While simple stacking of conventional chips increases packing density and reduces form factor, particularly for memory devices, the need for greater heterogeneous integration for mobile and other applications requiring very high packing density is driving the industry towards the use of full three dimensional (3D) packaging in which individual chips, thinned to < 100 μm, have interconnect on both front and back sides which are connected together using through silicon vias (TSVs). Typically these TSVs are filled with copper, which has a temperature coefficient of expansion (TCE) much greater than that of silicon, and therefore poses a risk of undesired stress generation in the thin silicon device layers with a potential adverse impact on device performance and reliability [1-4].

In this paper, we have studied the stress distribution in Si surrounded by TSVs, with various dimensions and pitches, to understand the potential impact of TSV layouts on device performance and reliability. The stress measurement and stress mapping was done using a fully automated, polychromator-based, multi-wavelength Raman spectroscopy system (MRS-300) designed for in-line process and material property monitoring applications by WaferMasters.

2. Experiment

200mm diameter Si wafers with various TSV diameters and layouts are prepared. The TSV diameters are varied from 20μm to 60μm and filled with Cu plugs. Details of the fabrication technology can be found in references 5 & 6. Three different pitches (1:2, 1:3 and 1:4) of TSV chains are fabricated for each TSV diameters. Figure 1 shows the TSV test chip wafer map and major TSV distribution maps used in this study.

Microscopic Raman spectroscopy is a very powerful, non-destructive characterization technique for crystallinity and stress/strain of semiconductor materials. Intensity, shift, and full width at half maximum (FWHM) of Raman signals are measured and analyzed to deduce valuable insights into many important physical characteristics of the materials [7]. Since Raman probing (penetration) depth is excitation wavelength dependent, multi-wavelength excitation capability is highly desired and gives important additional insights.

In this study, the MRS-300 system was used. Design concept and other details of the MRS-300 system can be found in other publications [8-9]. The system has three thermoelectrically cooled, charge coupled device (CCD) cameras that can measure Raman peaks from three different excitation wavelengths without any disruption (ie, without scanning the monochromator or switching the excitation laser). Three major spectral lines (457.9, 488.0 and 514.5nm) from a multi-wavelength Ar^+ ion laser are used as the excitation light source to collect Raman signals from different depths. The measurement capability of the system is summarized in Fig. 2.

3. Raman Results and Discussions

Stress free silicon exhibits a sharp and strong Raman peak corresponding to the optical phonon frequency at ~520.3cm^{-1} regardless of excitation wavelength. It is well known that the shift of Raman peak position towards the higher wavenumber side is proportional to the amount of compressive stress in Si. Compressive stress of ~434MPa causes 1.0 cm^{-1} shift of the Raman signal from Si towards the higher wavenumber side. The magnitude of compressive stress at the measurement point in Si can be estimated by multiplying 434MPa by the increase in Raman shift from the stress free Raman peak position.

Figure 3 summarizes the Raman shift and FWHM of line scan spectra from Si regions surrounded by 20μm diameter TSVs under 457.9, 488.0 and 514.5nm excitation. The line scan measurement was done in 2μm intervals. As measurement points moves away from the TSVs, the compressive stress of the Si becomes smaller, and some areas in the middle even develop tensile stress. While general trends are maintained in both lateral and depth directions, significant variations in stress value (Raman shift) and crystallinity (FWHM) are present in micron scale.

Figure 4 shows area maps of shift, FWHM and intensity of the Raman signal from Si surrounded by 20μm diameter TSVs. The intensity of Raman signals is strongest near the TSVs. Stress (Raman shift) and crystallinity (FWHM) of Si between TSVs show very large variations (±80MPa) and position dependence, related to the distance from neighboring TSVs.

We have confirmed that there is a strong dependence of TSV dimensions and layouts in stress distribution of Si, in both lateral and depth directions. Significant stress increase is expected in Si surrounded by high density, small diameter TSVs and may cause device performance variations and reliability issues.

4. Summary

It has been speculated that Si near TSVs are under compressive stress and that stress levels might be different depending upon TSV dimensions and layouts. Even though stress is often

considered to be one of suspicious factors for device reliability problems, there has been no direct and easy way to characterize stress in small scale devices. We have demonstrated stress mapping of Si surrounded by TSVs using the MRS-300 multi-wavelength Raman system. The Raman stress mapping with stress simulation can enhance our understanding of the impact of TSV dimensions and layouts on Si stress and stress induced device reliability problems.

References

[1] K.H. Lu et al, Proc. 59th Electronic Components and Technology Conf., San Diego, CA, 2009, 630.

[2] X. Liu et al, Proc. 59th Electronic Components and Technology Conf., San Diego, CA, 2009, 624.

[3] C.S. Selvanayagam et al, IEEE Transactions on Advanced Packaging, 32 (4), 2009, 720.

[4] C.S. Selvanayagam et al, Proc. 59th Electronic Components and Technology Conf., San Diego, CA, 2009, 612.

[5] X. Zhang et al, Proc. 59th Electronic Components and Technology Conf., San Diego, CA, 2009, 305.

[6] V.S. Rao et al, Proc. 59th Electronic Components and Technology Conf., San Diego, CA, 2009, 431.

[7] H. Harima, Proc. 14th IEEE Int. Conf. on Advanced Thermal Processing of Semiconductors, RTP 2006, (2006) 117.

[8] W.S. Yoo et al, Ext. Absts. Int. Conf. on Solid State Devices and Materials (2008) 376.

[9] W.S. Yoo et al, Appl. Phys. Exp. 2 (2009) 116502.

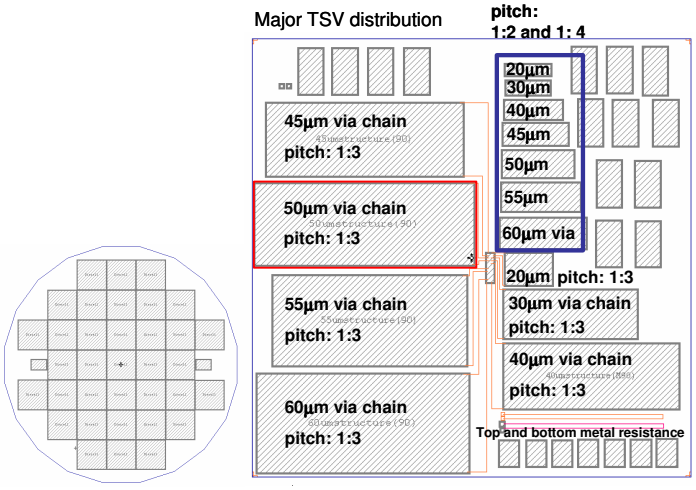

Fig. 1. Schematic illustration of a TSV test chip wafer map and major TSV distribution maps in individual test chips used in this study.

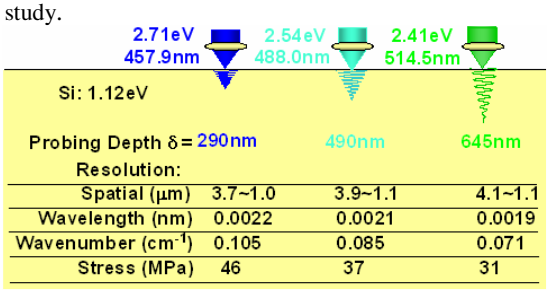

Fig. 2. Measurement capability of the MRS-300 with various excitation wavelengths from a multi-wavelength Ar^+ laser.

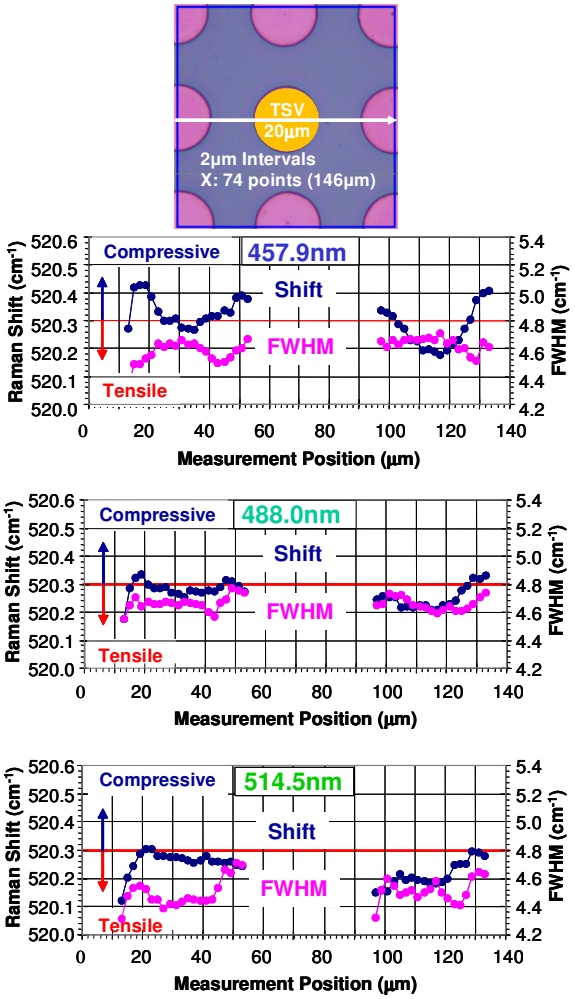

Fig. 3. Multi-wavelength line scan summary of Raman shift and FWHM of Si region between 20μm diameter Cu filled TSVs.

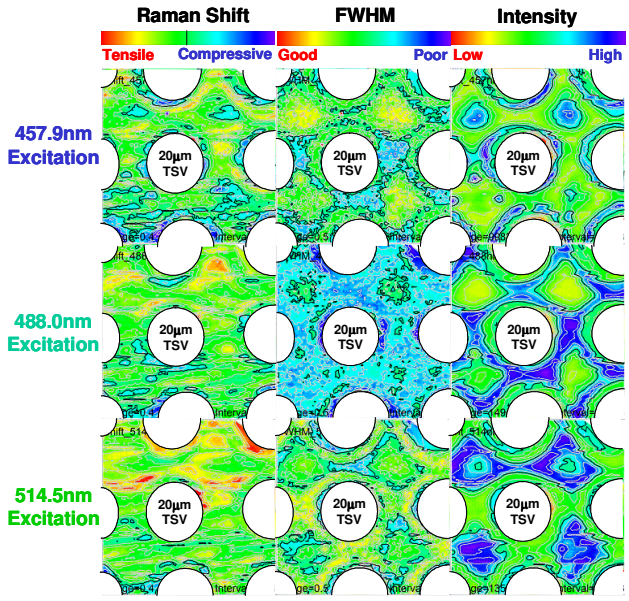

Fig. 4. Multi-wavelength area map summary of Raman shift, FWHM, and intensity in Si surrounded by 20μm diameter Cu filled TSV matrix.