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Above-CMOS Metal-Pattern Technique for Flexible Inductance Adjustment in Rapid Prototyping of RF SoCs

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1. Introduction

Mixed-signal SoCs, where radio frequency (RF) and/or analog front-end circuits are integrated with large-scale digital circuits, have become common. In RF circuit design, however, the estimation accuracy of RF circuit characteristics is not enough as compared with that in digital counterpart due to the severe effect of parasitic components. In the case of on-chip inductor design, for instance, magnetic field spreads widely and the characteristics of the inductor are affected by the substrate, passivation layer, surrounding metal patterns, etc. Furthermore, the interference between RF/analog and digital blocks is difficult to evaluate in design stage with reasonable simulation time and accuracy. If the measurement results of a test chip do not meet specifications, redesign and reproduction are inevitable. Therefore, not only a long period but also a high cost is required in the development of mixed-signal SoCs.

We have developed a novel prototyping method using above-CMOS inductor formation to solve the above-mentioned problems [1, 2]. In this method, a spiral inductor is formed on a fabricated and diced CMOS chip. Since the fabrication of above-CMOS passives is carried out in a chip-by-chip manner with simple processes, the flexible adjustment of the characteristics of passives and the evaluation of the chip performance can be carried out within a short turnaround time (TAT). Therefore, a cost-effective rapid prototyping of mixed-signal SoCs can be realized. Two types of above-CMOS inductor formation methods, namely, "*etching only*" method and "*deposition and etching*" method have been proposed [1, 2]. The former method uses blank top-metal-layer for creating spiral inductors by etching. Processing is very simple, but this method cannot be applied to the copper interconnect technologies. The later method uses additional aluminum layer newly deposited on the passivation layer of the chips. Very flexible modification of the inductor characteristics is possible at the sacrifice of increased processing cost. These two methods, however, have severe limitation. Inductor characteristics can not be evaluated before above-CMOS processing. In addition, CMOS chip design must be done supposing the above-CMOS processing beforehand. These drawbacks spoil the effectiveness of the method in prototyping.

In order to solve the problem, we have developed novel above-CMOS processing scheme which can modify the on-chip inductor characteristics using parasitic metal pattern formation on the passivation layer above the on-chip inductor.

2. Above-CMOS Metal Pattern for Modifying Inductance

Figure 1 shows the concept of the proposed method. Same as the conventional prototyping, an on-chip spiral inductor and related RF circuit performance are evaluated by an on-chip probing after a normal CMOS manufacturing process. If there is discrepancy between expected and measured results, above-CMOS processing is made on a chip separately to adjust the inductor parameters of each chip. The above-CMOS processing is carried out as follows. An additional metal layer is first deposited on the passivation layer and then patterned into various shapes to modify the inductor characteristics. If measured results are still imperfect, further cut-and-try trials can be carried out many times within a short TAT.

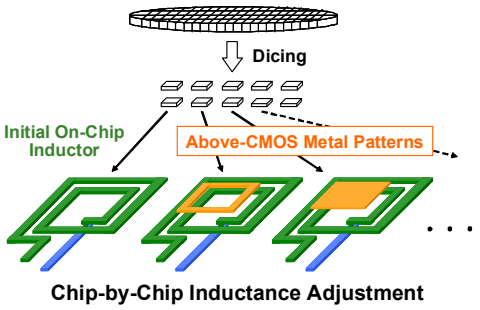

Fig. 1 Concept of the Above-CMOS processing for inductance adjustment.

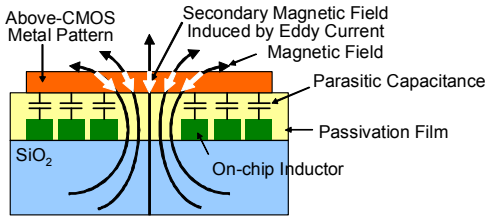

Fig.2 Mechanism of the inductor characteristics modification by the above-CMOS parasitic metal pattern formations.

Figure 2 schematically shows the mechanism of the inductor characteristics modification by the above-CMOS parasitic metal pattern formations. When the metal pattern is placed on the on-chip inductor, alternating magnetic field piercing the metal plate induces eddy current and it disturbs the magnetic field, resulting in the decrease in the inductance. At the same time, parasitic capacitive coupling between the spiral inductor pattern and the metal pattern increases the parallel capacitance of the inductor, resulting in the decrease in the self-resonant frequency SRF and effective increase in inductance at the frequency below SRF. Therefore, various metal patterns controlling eddy current flow and parasitic capacitance can modify the effective inductances of the on-chip inductor.

3. Results and Discussion

Figure 3 shows photomicrographs of various metal

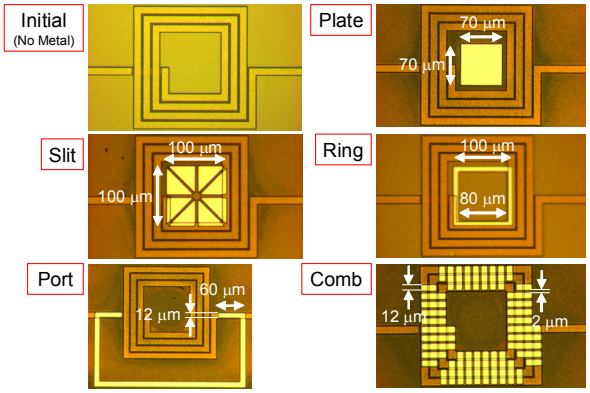

Fig. 3 Various above-CMOS metal patterns evaluated in this study.

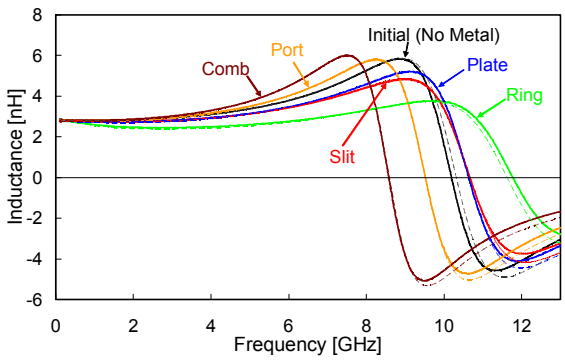

Fig. 4 Inductance modifications by above-CMOS metal patterns. Measured and modeled results are shown in solid and dashed lines, respectively.

patterns evaluated in this study. Fabrication process steps are as follows. CMOS chips having on-chip inductors were fabricated with the conventional 0.18 µm CMOS process. A fabricated and diced 5 x 5 mm^2 CMOS chip was pasted on a 2" silicon wafer for easy handling in later processes. After 1-µm thick aluminum thin-film deposition by sputtering, various shapes were patterned by one-time photolithography using a parallel light aligner (2 µm rule). Note that laser beam direct writing technology may be applied as a more effective patterning method. Then the etching of the deposited aluminum layer completes the processing. Since patterns are large and no electrical contact to the underlying circuits is needed, processing can be very simple and low-cost.

Figure 4 shows measured inductances of the on-chip inductors with above-CMOS metal patterns. In the "Plate," "Slit" and "Ring" cases, inductances at the frequencies around few GHz range decreased. On the other hand, inductances increased in the "Port" and "Comb" cases at the sacrifice of SRF reduction. It is experimentally verified that the developed scheme can both increase and decrease the inductance with a very simple above-CMOS processing. Variation range of inductance measured at 2.4 GHz, which is little below the frequency exhibiting peak quality factor Q, was -14 to +2.5%. Quality factor Q, however, decreases in all cases.

The developed inductance adjustment method has been applied to the LC-VCO design as shown in Fig. 5. Oscillation frequency has been modified in this scheme.

The change in inductor characteristics caused by above-CMOS metal patterns can be expressed well by the

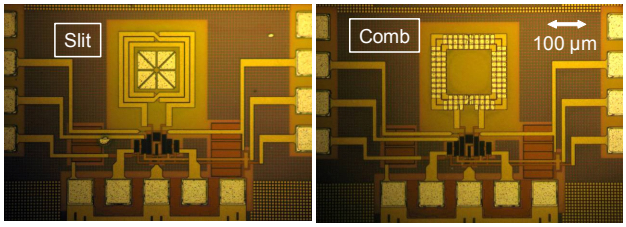

Fig. 5 LC-VCOs using above-CMOS inductor tuning.

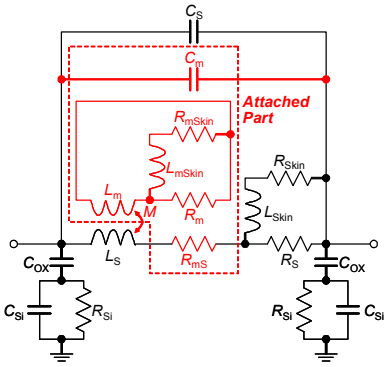

Fig. 6 Newly developed inductor model, which is applicable to the above-CMOS inductor tuning.

newly developed inductor model shown in Fig. 6. With the attachment of the mutual inductance coupling part composed of an LR-ladder components and parallel parasitic capacitance to the original π-model of an on-chip inductor, the characteristics of the inductor with the above-CMOS metal pattern at the frequency below SRF can be expressed with sufficient accuracy as shown in Fig. 4 by dashed lines. Note that the characteristics changes in L and Q caused by various metal patterns examined here can be fully expressed by tuning the parameters of the attached part alone and the remaining parameters of the original π-model can be left as they are for the on-chip inductor. This successful modeling can ease the redesign of the on-chip inductor for the final product even when it is required.

4. Conclusion

Very simple yet flexible inductance adjustment scheme has been developed using above-CMOS metal pattern formation. Measurement results showed that the above-CMOS simple processing with chip-by-chip manner can both increase and decrease the on-chip inductances by modifying planar patterns of metal layer deposited on the passivation-layer. It is thus concluded that the rapid prototyping of RF-SoCs can be realized by this method. This cut-and-try based method is a realization of a "breadboard" technology on an LSI chip.

Acknowledgement

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References

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