Above-CMOS Metal-Pattern Technique for Flexible Inductance Adjustment in Rapid Prototyping of RF SoCs

Koji Kotani, Atsuo Sugimoto, Yutaka Omiya, and Takashi Ito

Department of Electronics, Graduate School of Engineering, Tohoku University
6-6-05 Aza-Aoba, Aramaki, Aoba-ku, Sendai 980-8579, Japan
Phone: +81-22-795-7122, Fax: +81-22-263-9396, E-mail: kotani@ecei.tohoku.ac.jp

1. Introduction

Mixed-signal SoCs, where radio frequency (RF) and/or analog front-end circuits are integrated with large-scale digital circuits, have become common. In RF circuit design, however, the estimation accuracy of RF circuit characteristics is not enough as compared with that in digital counterpart due to the severe effect of parasitic components. In the case of on-chip inductor design, for instance, magnetic field spreads widely and the characteristics of the inductor are affected by the substrate, passivation layer, surrounding metal patterns, etc. Furthermore, the interference between RF/analog and digital blocks is difficult to evaluate in design stage with reasonable simulation time and accuracy. If the measurement results of a test chip do not meet specifications, redesign and reproduction are inevitable. Therefore, not only a long period but also a high cost is required in the development of mixed-signal SoCs.

We have developed a novel prototyping method using above-CMOS inductor formation to solve the above-mentioned problems [1, 2]. In this method, a spiral inductor is formed on a fabricated and diced CMOS chip. Since the fabrication of above-CMOS passives is carried out in a chip-by-chip manner with simple processes, the flexible adjustment of the characteristics of passives and the evaluation of the chip performance can be carried out within a short turnaround time (TAT). Therefore, a cost-effective rapid prototyping of mixed-signal SoCs can be realized. Two types of above-CMOS inductor formation methods, namely, "etching only" method and "deposition and etching" method have been proposed [1, 2]. The former method uses blank top-metal-layer for creating spiral inductors by etching. Processing is very simple, but this method cannot be applied to the copper interconnect technologies. The later method uses additional aluminum layer newly deposited on the passivation layer of the chips. Very flexible modification of the inductor characteristics is possible at the sacrifice of increased processing cost. These two methods, however, have severe limitation. Inductor characteristics can not be evaluated before above-CMOS processing. In addition, CMOS chip design must be done supposing the above-CMOS processing beforehand. These drawbacks spoil the effectiveness of the method in prototyping.

In order to solve the problem, we have developed novel above-CMOS processing scheme which can modify the on-chip inductor characteristics using parasitic metal pattern formation on the passivation layer above the on-chip inductor.

2. Above-CMOS Metal Pattern for Modifying Inductance

Figure 1 shows the concept of the proposed method. Same as the conventional prototyping, an on-chip spiral inductor

3. Results and Discussion

Figure 3 shows photomicrographs of various metal
A fabricated and diced 5 x 5 mm² CMOS chip was pasted on a fabricated with the conventional 0.18 µm CMOS process. A as follows. CMOS chips having on-chip inductors were patterns evaluated in this study. Fabrication process steps are above-CMOS metal patterns can be expressed well by the Oscillation frequency has been modified in this scheme. Applied to the LC-VCO design as shown in Fig. 5.

Variation range of inductance measured at 2.4 GHz, which is inductances increased in the "Port" and "Comb" cases at the frequencies around few GHz range decreased. On the other hand, inductances increased in the "Port" and "Comb" cases at the sacrifice of SRF reduction. It is experimentally verified that the developed scheme can both increase and decrease the on-chip inductances by modifying planar patterns of metal layer deposited on the passivation-layer. It is thus concluded that the rapid prototyping of RF-SoCs can be realized by this method. This cut-and-try based method is a realization of a "breadboard" technology on an LSI chip.

4. Conclusion
Very simple yet flexible inductance adjustment scheme has been developed using above-CMOS metal pattern formation. Measurement results showed that the above-CMOS simple processing with chip-by-chip manner can both increase and decrease the on-chip inductances by modifying planar patterns of metal layer deposited on the passivation-layer. It is thus concluded that the rapid prototyping of RF-SoCs can be realized by this method. This cut-and-try based method is a realization of a "breadboard" technology on an LSI chip.

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References