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Improvement of High-k/metal gate pMOSFET performances and reliability with optimism Si cap/SiGe channel structure

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1. Introduction

We report the optimism channel stack ratio by controlling strained SiGe and Si cap layer thickness to overcome Ge diffusion and confine carriers in strain SiGe layer without forming a significant parasitic channel at the interface. With the optimized channel structure, performances (high mobility and driving current) Hf-based high-k/metal gate SiGe pMOSFET with appropriate V_{TH} [~ -0.3V], low C-V hysteresis (< 5mV), superior Ion-Ioff, V_{TH} roll-off, V_{TH} stability and comparable NBTI and HCI reliability was achieved.

2. Experiments

SiGe channel pMOSFETs were fabricated using a 32nm high-k/metal gate-first CMOS process flow. Thin strained $Si_{0.75}Ge_{0.25}$ with thickness 5 to 8 nm epi-layers were grown and different Si capping layers (4 ~ 7 nm) were sequentially deposited. A SiO_2 interfacial layer (IL) was formed before high-k layer. Hf-based oxide was deposited by atomic layer deposition (ALD) method. After the gate stack formation with a TiN metal electrode, a laser spiking annealing and standard backend integration was employed (Fig. 1).

3. Results and Discussions

The SiGe layer on Si substrate provides a compressive strain. [1~3] Excellent Ion-Ioff performance were obtained with thickness ratio = 0.9 (Si cap/SiGe = 4.6/5 nm), as shown in Fig. 2. Improper thickness ratio = 0.6 (Si cap/SiGe = 4.6/8 nm) in which Si cap is too thin to suppress Ge diffusion. [4] If Si cap is too thick (thickness ratio = 1.3, Si cap/SiGe = 6.6/5 nm), higher voltage drop on it will produce a parasitic channel at the interface. [5] Fig. 3 shows the appropriate V_{TH} and minimum V_{TH} roll-off characteristic were achieved with thickness ratio = 0.9 by the modulation of channel band gap rather than relying on metal work function. V_{TH} stability will be degraded with improper thickness ratio = 0.6, as shown in Fig. 4. Because of above, we found Si cap/SiGe channel stack ratio 0.8 and 0.9 (especially 0.9) have better performance than others. Therefore, we focus on two Si cap/SiGe channel structure (Si cap/SiGe = 4.6/5 or 6.6/8 nm) and investigate performance and reliability comprehensively with Si channel to find the optimism thickness ratio. Due to the strain induced reduction of the holes effective mass and splitting of heavy and light holes band, SiGe pMOSFET have behaved higher holes mobility and driving current compared to Si channel device [6~7] especially with optimized SiGe channel stack ratio = 0.9, as shown in Fig. 5 and 6. However, buried channel device have worse gate control ability, slighter degradation in the subthreshold swing of SiGe device can be found (Fig. 7). By introduction of strained SiGe layer doesn't degrade equivalent oxide thickness (EOT), as shown in Fig. 8. The hysteresis instability also can be improved with optimized Si cap/SiGe channel structure. Therefore, with careful control Si cap/SiGe layer thickness, carriers can be confined effectively in the strained SiGe layer and the interface defect induced by carrier injection can also be minimized.

Fig. 9 and 10 show the I_D degradation of Hf-based high-k/metal gate device after NBTI and HCI inspection. SiGe pMOSFETs have less I_D degradation than control Si device especially with optimized SiGe channel structure. By introduction of strained SiGe layer, the holes are primarily located in the SiGe channel due to valence band offset and thus the holes concentration in Si surface channel is lower than that of control Si pMOSFET. Besides, the hot carriers of the buried channel device have to travel a longer distance to reach the Si/SiO_2 interface, and therefore, suffer more energy-robbing collision. [8] With optimized Si cap/SiGe layer thickness ratio, carriers can be confined effectively in the strained SiGe layer. So the SiGe pMOSFETs with lower concentration at interface can improve NBTI effect. [8] Moreover, this would decrease the number of carrier that has enough energy to surmount the Si/SiO_2 potential barrier. Thus, the hot carrier effect is also reduced. We then use TCAD simulation to inspect holes and total current distribution in Fig. 11 and Fig. 12. We can found carriers and current confined effectively in strain SiGe layer in thickness ratio = 0.9. Therefore, with carefully control Si cap/SiGe channel stacks, carriers can be confined effectively in the strained SiGe layer without formation of a significant parasitic channel at the interface.

4. Conclusions

In this work, we find the optimism Si cap/SiGe layer thickness ratio is the best trade-off between a good interface quality and confinement of carrier in the strained SiGe layer. This optimism thickness ratio paves the way for high performance and better reliability high-k/metal gate SiGe pMOSFET at future technology nodes.

Acknowledge

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References

[1] H. R. Harris *et al.., VLSI* 2007. pp. 154-155.
[2] J. M. Hinckley *et al.,APL* 1989. pp. 2008-2010.
[3] S. L. Wu *et al., Semicond. Sci. Technol*, 2005. pp. 559-562.
[4] S. Suthram. *et al., IEDM 2007*. pp. 727-730.
[5] S. L. Wu *et al., APL 1999*. pp. 2848-2850.
[6] J. M. Hinckley *et al., Phys. Rev. B* 1990. pp. 2912-2926.
[7] Z. Shi *et al., Appl. Surf. Sci* 2004. pp. 248-253.
[8] S. Tam *et al., IEEE Trans. Electron Devices* 1984. pp. 1116-1125.

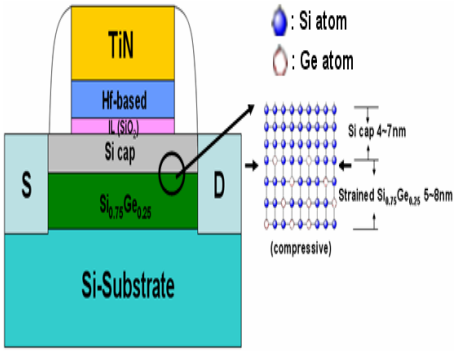

Fig.1. The schematic illustration of the Hf-based high-k/metal gate SiGe pMOSFET structure.

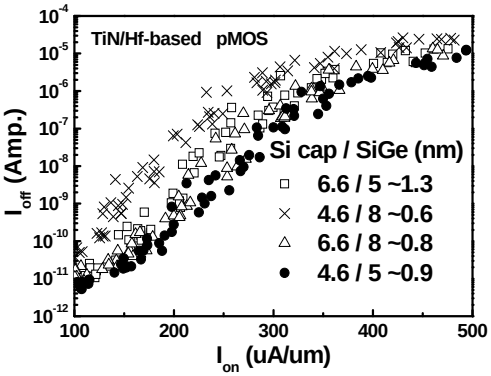

Fig.2. Excellent Ion-Ioff performance and higher driving capability increase were obtained with thickness ratio = 0.9 (Si cap/SiGe = 4.6/5 nm).

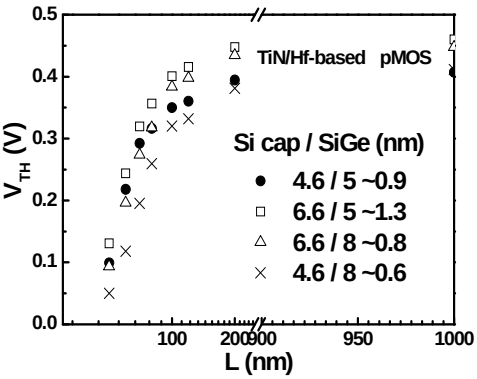

Fig.3. Appropriate V_{TH} and minimum V_{TH} roll-off characteristic was achieved with thickness ratio = 0.9 (Si cap/SiGe = 4.6/5 nm).

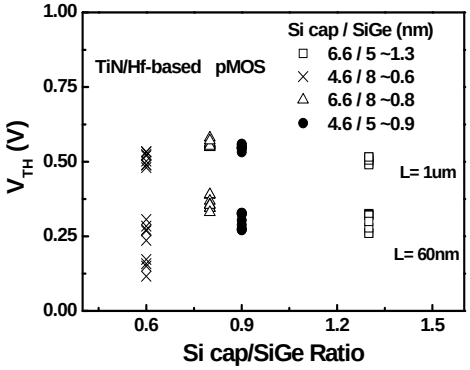

Fig.4. V_{TH} stability will be degraded with improper thickness ratio = 0.6 (Si cap/SiGe = 4.6/8 nm) which can not suppress Ge diffusion.

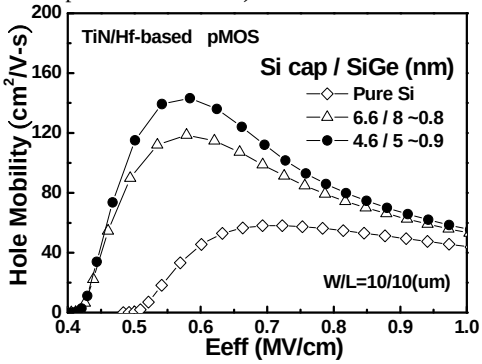

Fig.5. Higher holes mobility can be obtained by optimized SiGe channel stack ratio = 0.9 (Si cap/SiGe = 4.6/5 nm).

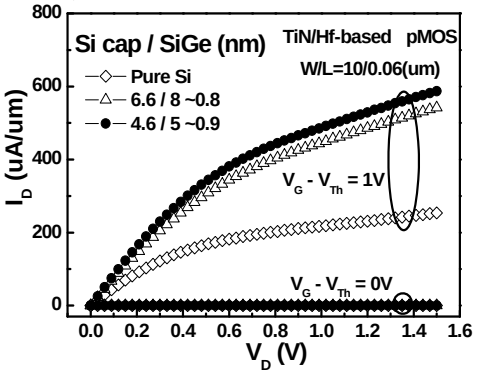

Fig.6. Better driving capability can be obtained with optimized SiGe channel stack ratio = 0.9 (Si cap/SiGe = 4.6/5 nm).

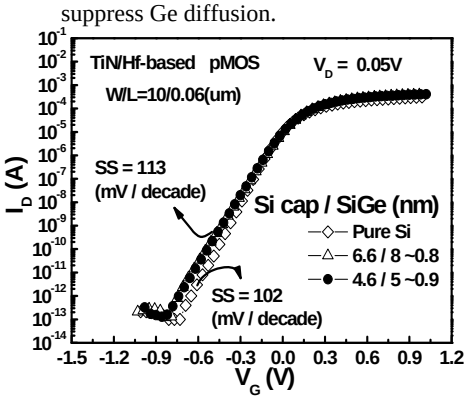

Fig.7. Buried channel device have worse gate control ability, slighter degradation in the subthreshold swing of SiGe device can be found.

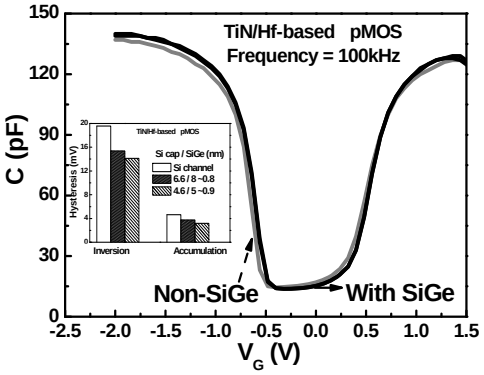

Fig.8. By introduction of strained SiGe layer in pMOSFET doesn't degrade EOT and hysteresis instability can be improved with optimized Si cap/SiGe channel structure.

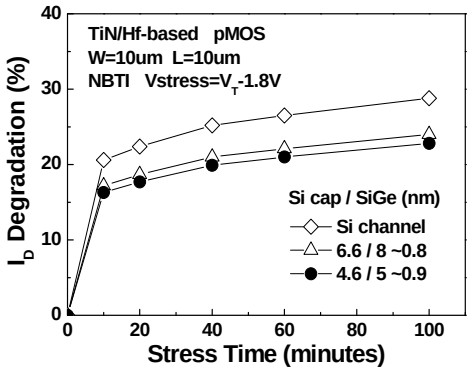

Fig.9. SiGe pMOSFETs have less I_D degradation than control Si device after NBTI inspection especially with optimized SiGe channel stack ratio = 0.9 (Si cap/SiGe = 4.6/5 nm).

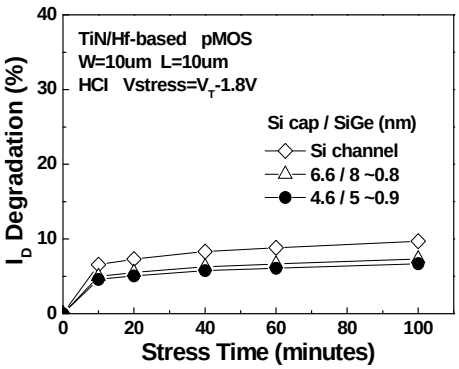

Fig.10. SiGe devices have less I_D degradation than control Si device after HCI test especially with optimized SiGe channel stack ratio = 0.9 (Si cap/SiGe = 4.6/5 nm).

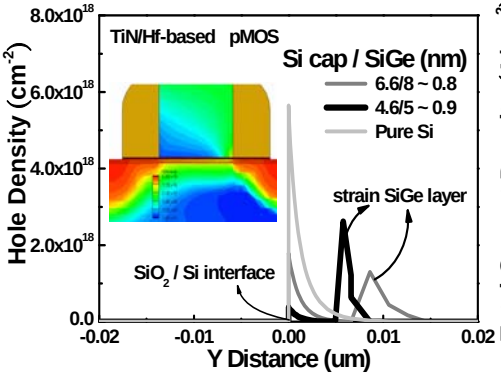

Fig.11. Holes confined effectively in strain SiGe layer with optimized thickness ratio = 0.9 (Si cap/SiGe = 4.6/5 nm) by TCAD simulation.

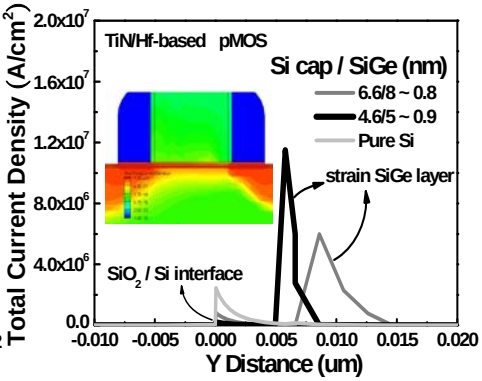

Fig.12. Total current confined effectively in strain SiGe layer with optimized thickness ratio = 0.9 (Si cap/SiGe = 4.6/5 nm) by TCAD simulation.