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Investigation of Low-Cost Stress Memorization Process on Layout and Low-Frequency Noise Performance for Strained-Si nMOSFETs

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1. Introduction

The use of strained Silicon technologies has become requisite to satisfy the aggressive performance targets of new device technology nodes. Recently, low-cost stress memorization technique (SMT) has been reported to further boost nMOSFETs performance [1-2]. However, the layout effects of SMT devices are still not clear and merits further investigation. On the other hand, low frequency (1/*f*) noise measurements also yield information about the quality of the gate oxide [3], contacts, and might be also used for studying degradation processes. Hence, the 1/*f* noise analysis can be used as a diagnostic tool for the SMT process. In this work, we try to observe the SMT-induced tensile strain dependence on layout effects and 1/*f* noise behavior of the SMT process.

2. Experiment

The nMOSFETs used in this study were fabricated by state-of-the-art low-cost stress memorization technique CMOS process [4]. Additionally, Fig. 1 shows the device's layout parameters.

3. Results and Discussion

I_{on}-I_{off} curve of n- and pMOSFETs for control and SMT devices are illustrated in Fig. 2 and Fig. 3, respectively. An 8% I_{on} improvement at I_{off} = 10^{-7} A/μm was obtained for SMT nMOSFETs, as compared to control nMOSFETs, showing the SMT process indeed induce additional tensile stress in the channel. No degradation is observed for pMOSFETs in Fig. 3. This is due to non-sensitive piezoresistance coefficients observed in (100)/<100> pMOSFET [5]. The drain current (I_D) of control and SMT devices on the poly spacing and length of source/drain ($L_{S/D}$) are shown in Fig. 4 and Fig. 5, respectively. It was found that the I_D decreased as poly spacing and $L_{S/D}$ scaled down. This is attributed to the tensile strain transfer into channel become insufficient. At the same time, the I_D of SMT devices decreased rapidly at poly spacing below 0.2 μm and $L_{S/D}$ below 0.5 μm was observed. It also implies that the additive strain created in the source/drain diffusion region is the primary stress-induce mechanism by SMT process. This conclusion is similar to the data demonstrated in previous studies on SMT [2]. Besides, further examine the strain effects of SMT along gate width direction is also provided. The relationship between gate width (W) and I_D is evaluated, as shown in Fig. 6. It can be seen that the I_D of SMT devices higher than control devices due to additive SMT-induced tensile strain increase carrier mobility. To clarify the origin of mobility enhancement, the total resistance (R_{tot} = R_{ch} + R_{SD}) of different W versus gate length is plotted in Fig. 7, in which the carrier mobility from the reciprocal of slope can be observed [7]. It indicates that the reduction W can effectively enhance carrier mobility. It could be attributed the increase of tensile stress along channel width direction [8]. Furthermore, it is also found that the strain effects of SMT and strain contact etch stop layer (CESL) are similar as W scaled down.

To analyze 1/*f* noise behavior for both devices, we measured large area devices in order to focus on SMT process. The drain current noise (S_{ID}) versus frequency for both devices is shown in Fig. 8. The spectra show typical $1/f^{\gamma}$ noise type with the frequency exponent γ close to one. Fig. 9 shows the S_{ID} at *f* = 10 Hz versus I_D for the both devices. It can be seen that the increasing S_{ID} with I_D^2 (for I_D < ~10^{-5}A) indicated a carrier number fluctuations dominated 1/*f* noise. As I_D > 10^{-5}A, the increasing S_{ID} with I_D^1 implied that carrier number fluctuations may correlate mobility or source/drain series resistance fluctuations. To further exclude source/drain series resistance influence of 1/*f* noise source, the normalized drain current noise S_{ID}/I_D^2 at *f* = 10 Hz versus the gate overdrive voltage was shown in Fig. 10. As seen $S_{ID}/I_D^2 \sim (V_{GS}-V_{TH})^{-1}$ as it should be for the 1/*f* noise originated from the channel [6]. The results confirmed that the carrier number correlated mobility fluctuations (unified model) for 1/*f* noise in both devices. The unified model mechanism is also further illustrated in Fig. 11 and Fig. 12. Fig. 11 shows S_{ID}/I_D^2 and $(g_m/I_D)^2$ versus I_D for both devices. The S_{ID}/I_D^2 exhibits a fairly good proportionality with $(g_m/I_D)^2$. In addition, the associated input-referred voltage spectral noise (S_{VG} = S_{ID}/g_m^2) shows a parabolic dependence with gate voltage at strong inversion (Fig. 12). These results also point to that the 1/*f* noise can be reasonably interpreted by the unified model [3]. Moreover, the values of the S_{ID}/I_D^2 and S_{VG} for both devices are similar. It can be reasonably attributed to the lower concentration of hydrogen for SMT stack process, which brought out the comparable 1/*f* noise level between both devices [9].

4. Conclusions

It was observed that the SMT-induced tensile strain created in the source/drain region is the primary origin. The DC characteristics of the SMT devices are more sensitive to layout, as the device is scaled down. Moreover, it was found

that the mechanism of 1/*f* noise in both devices can be properly interpreted by the unified model. Furthermore, SMT devices showed comparable noise level to the control device, indicating that the SMT process will not degrade interface quality.

Acknowledgements

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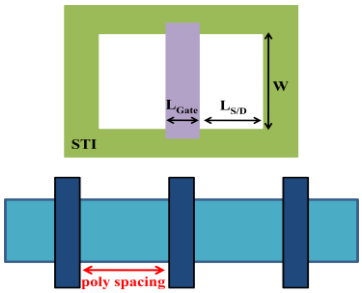

Fig. 1 Schematic of device's layout parameters.

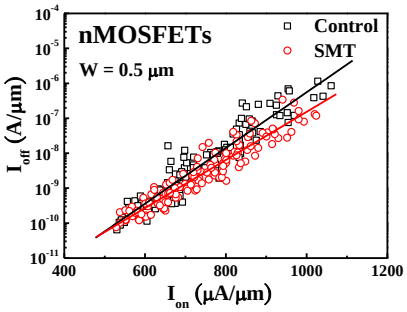

Fig. 2 I_{on}-I_{off} curve of control and SMT nMOSFETs.

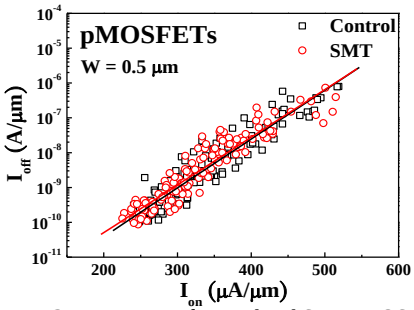

Fig. 3 I_{on}-I_{off} curve of control and SMT pMOSFETs.

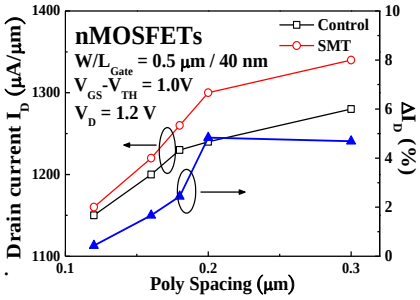

Fig. 4 Drain current for various poly spacing under V_{GS}-V_{TH}= 1.0 V and V_{DS} = 1.2V.

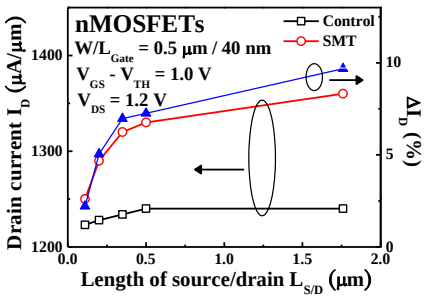

Fig. 5 The drain current (I_D) for both nMOSFET with various length of source/drain ($L_{S/D}$).

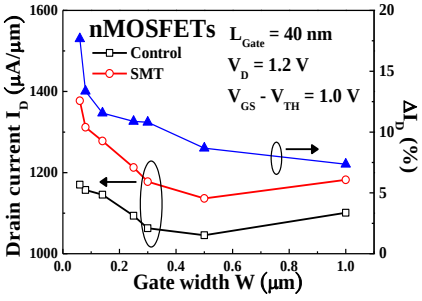

Fig. 6 Dependence of I_D on gate width (W) for SMT device and the control device.

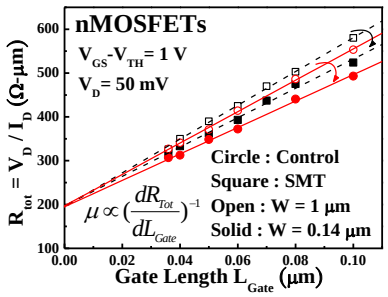

Fig. 7. Total resistance of different W for control and SMT nMOSFETs as function of the gate length.

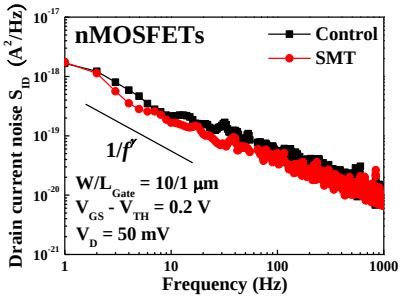

Fig. 8 drain current noise (S_{ID}) versus frequency for both devices at $V_{GS} - V_{TH}$ =0.2 V.

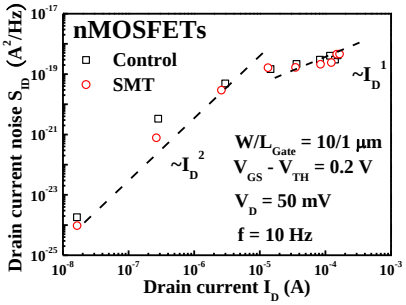

Fig. 9 The drain current noise (S_{ID}) versus frequency for both devices.

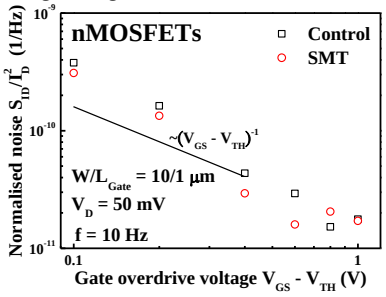

Fig. 10 dependence of the normalized drain current noise S_{ID}/I_D^2 on the gate overdrive voltage swing.

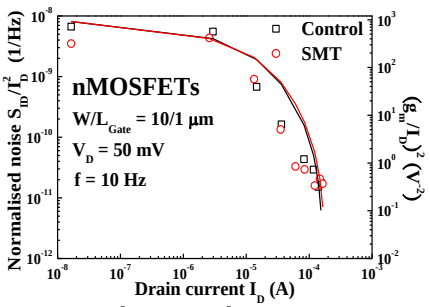

Fig. 11 S_{ID}/I_D^2 and $(g_m/I_D)^2$ versus I_D for both devices.

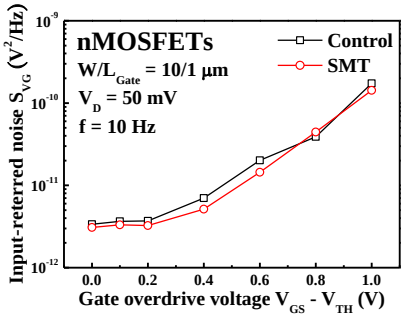

Fig. 12 Input-referred voltage spectral noise (S_{VG} = S_{ID}/g_m^2) versus V_{GS} - V_{TH} for both devices