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# Characterization the random telegraph noise in 32nm high-k/metal gate CMOSFETs

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## 1. Introduction

Random telegraph noise (RTN) is one of the most concerns in device scaling down. For the first time, the RTN of 32nm high-k/metal gate nMOSFETs and pMOSFETs have been investigated. The RTN fluctuation ($\triangle I_D$) in nMOSFETs is larger than it in pMOSFETs, especially for the short channel device. Besides, the traps leading to RTN were found in high-k layer ($HfO_2$) or in interfacial layer ($SiO_2$) using variable frequency charge pumping technique. Thus, we also investigated the relationship of RTN and defect traps in both high-k/metal gate nMOSFETs and pMOSFETs.

## II. Experiments

A 32-nm technology was used as a vehicle to demonstrate Hf-base gate CMOS process. For this experiment, we measure the $HfO_2$ device with the gate width of 0.25um and length of 200nm ~ 32nm. The gate stack consists of TiN electrode, $HfO_2$ 3nm as the high-k dielectric layer, and $SiO_2$ of 1nm as the IL. The RTN signal was measured by a fast I-V measurement unit (Agilent 1530A). The gate and drain electrodes are biased in variable voltage, while the source and substrate electrodes are grounded.

## III. Results and Discussions

Random telegraph noise, which is $I_D$ fluctuation induced by the stochastic trapping in the gate stack. It is the critical concerns in the present and future VLSI design because it unpredictably and greatly fluctuate the dynamic performance [1-3]. It is important to clarify the mechanism of RTN signal in NMOS and PMOS, to realize the trapping behaviors in the high-k gate device. In this paper, we present experiment evidence which indicates that the RTN fluctuation ($\triangle I_D$) nMOSFETs is severe than it in pMOSFETs, which is inducing by the bulk defects, expecially in 32 nm generation FETs and beyond.

Fig. 1 and Fig. 2 show the time domain $I_D$ RTN at various gate lengths. Gate width is fixed at 0.25um and gate length is varied from 200nm to 32nm. It can easily find that the RTN is getting a trouble by channel dimension scaling down both in nMOSFET and pMOSFET. This result is similar to the other study [4]. Besides, fig. 3 and fig. 4 show the maximum $\triangle I_D$ in nMOSFET is 8.1% and in pMOSFET is 6.2% at 32nm device, respectively. It represents that the $\triangle I_D$ in nMOSFET is larger than the pMOSFET due to the RTN stochastic defects trapping/detrapping. This result implies that a large number of RTN traps is easily found in the high-k nMOS gate dielectric, in other word, the $I_D$ variation should been considered more carefully in the next generation nMOSFETs high-k gate device. We can charily find the $I_D$ distribution is smoother in pMOS than in nMOS for 32nm device at fig. 5. Hence, it may suggest that the trap in pMOS is more uniform than it in nMOS at vertical direction for high-k gate stack. Following, noise of power spectrum density (PSD) and variable frequency charge pumping technique are used to investigate the traps depth profile [5][6].

The PSD shows the 1/f decay in the long channel device and $1/f^2$ decay in the short channel device both of the nMOSFETs and pMOSFETs in the fig. 6 and fig. 7. 32nm device has the worst RTN than long channel device and it's noise signal is closed to $1/f^2$ decay. From the RTN pathways through the dielectric in the fig. 8, it represents that if we want to detect the deeper trap, high sample rate should be used to measure the $I_D$ fluctuation which is induced by the bulk trapping/detrapping. Hence, when the PSD is more close to $1/f^2$ decay, RTN stochastic trapping is getting important and in the bulk dielectric. The PSD slope of 32nm is -1.85 of nMOSFETs and -1.62 of pMOSFETs in the table. 1, respectively. Compareing the impact with different gate length, the RTN noise can not be neglect in the 32nm device and nMOSFETs is severe than pMOSFETs. In the fig. 9, charge pumping (CP) measurements are conducted using typical conditions of 1MHz to 16kHz frequency range and 1V gate voltage swing to evaluate the traps depth profile. Fig. 10 and Fig. 11 show the trap profiles of nMOS and pMOS, respectively. The growing of defect trap in the nMOSFETs is faster than the pMOSFETs. It can also demonstrate that the penetration of electron traps in nMOSFETs is severer than hole traps in pMOSFETs. Besides, some paper pointed out that bulk trapping in the high-k is found to be the dominant mechanism responsible for nMOS PBTI, whereas pMOS NBTI degradation is interface drive [7]. High-k dielectric nMOSFETs shows severe PBTI (Positive-Bias Temperature Instability) than NBTI (Negative-Bias Temperature Instability) of pMOSFETs [8]. Therefore, we conclude that the RTN is causing the apparent $I_D$ variation issue in the 32nm generation and beyond which is inducing by the high-k bulk defect film and will also influence the critical PBTI reliability, especially for the nMOSFETs.

## VI. Conclusions

The RTN fluctuation in nMOSFETs is larger than that in pMOSFETs, especially with device scaling down. Noise of power spectrum density and variable frequency charge pumping technique were both used, and found the penetration of electron traps in nMOSFETs is severer than hole traps in pMOSFETs. Thus, drain current and reliability instability in 32nm and beyond nMOSFETs, should be considered more due to the RTN stochastic trapping in high-k bulk film.

### Acknowledge

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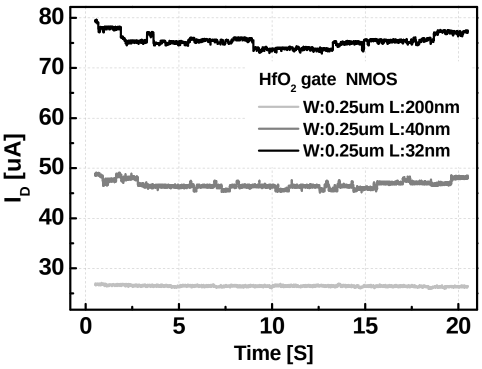


Fig.1. Time dependence of drain current ($I_D$) in the $HfO_2$ nMOSFET. Random telegraph noise (RTN) is clearly observed in the small device.

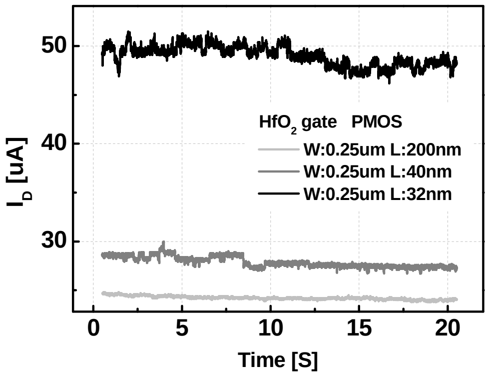


Fig.2. Time dependence of drain current ($I_D$) in the $HfO_2$ pMOSFET. Random telegraph noise (RTN) is clearly observed in the small device.

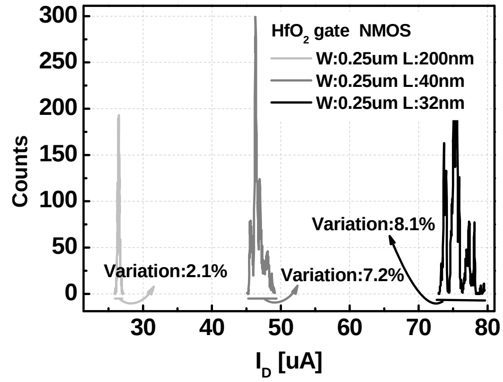


Fig.3. Distribution of drain current in the $HfO_2$ nMOSFET. $I_D$ variation apparently increases when device scaling down.

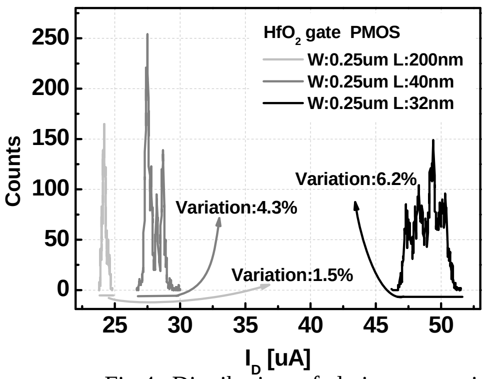


Fig.4. Distribution of drain current in the HfO2 nMOSFET. $I_D$ variation apparently increases when device scaling down.

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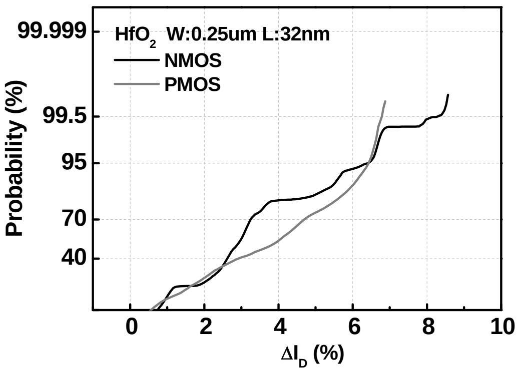


Fig.5. Probability for $\triangle I_D$ at $HfO_2$ gate in 32nm device. NMOSFET has larger $I_D$ variation than pMOSFET.

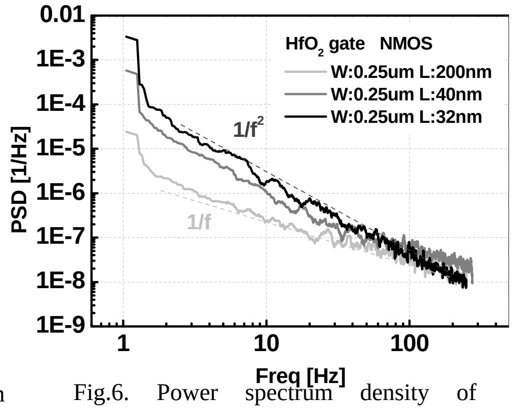


Fig.6. Power spectrum density of nMOSFET. $HfO_2$ device's PSD clearly shows the $1/f^2$ decay in 32nm gate length.

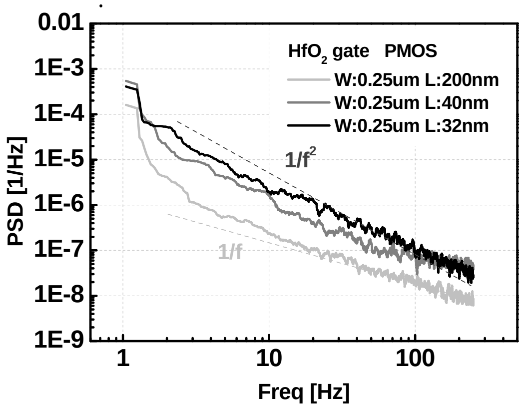


Fig.7. Power spectrum density of pMOSFET. HfO2 device's PSD forwards to the $1/f^2$ decay with gate length scaling down.

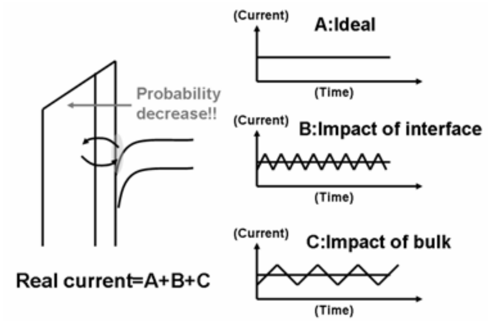


Fig.8. Schematic diagram illustrating the RTN pathways through the dielectric.

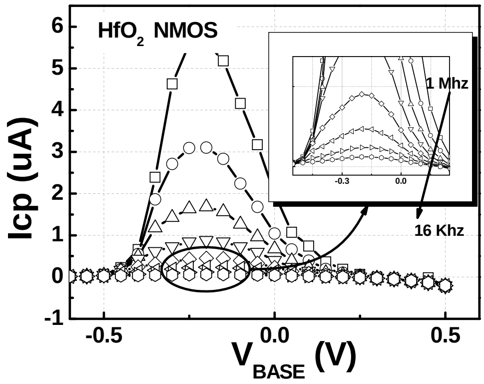


Fig.9. Charge pumping current for frequencies ranging from 8kHz to 1Mhz.

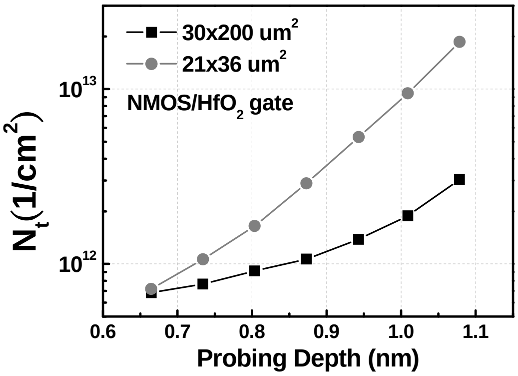


Fig.10. Charge pumping trap density versus probing depth in nMOSFET. As depth increases, trap density also increase.

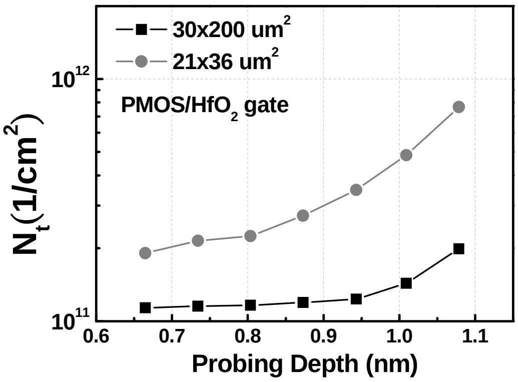


Fig.11. Charge pumping trap density versus probing depth in pMOSFET. Less trap density generation is detected with depth increases in pMOSFET.

| PSD slope | L:200 (nm) | L:40 (nm) | L:32 (nm) |
|---|---|---|---|
| nMOS | -0.9 | -1.3 | -1.85 |
| pMOS | -1.08 | -1.33 | -1.62 |

Table.1. PSD slope of nMOSFET is larger than pMOSFET in 32nm gate device. With device scale down, $1/f^2$ noise is getting important than 1/f noise.