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The Compact Modeling of Zero Temperature Coefficient (ZTC) Point of DTMOS

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Ⅰ. ABSTRACT

For the first time, the compact analytical expressions of zero-temperature-coefficient (ZTC) point modeling of DTMOS transistor are successfully presented in detail. Newly analytical formulations are developed for both linear and saturation regions of DTMOS transistor operation that ensure the drain current to be temperature independent for the optimal gate voltage. The maximum error of 0.87% and 2.35% in the linear and saturation regions confirms good agreement between our DTMOS ZTC point model and the experimental data, respectively. Compared to traditional MOSFET, the lower V_g(ZTC) with higher overdrive current of DTMOS improves the speed and efficiency of ICs for the low power consumption requirement in green CMOS technology.

Ⅱ. INTRODUCTION

The important parameter zero-temperature-coefficient (ZTC) point was well known for its stable CMOS integrated circuit work over an operated temperature. However, the ZTC point theory of DT technology [1]-[4] has not been derived in previous studies [5]-[6]. In this research, the ZTC design criterion for a stable integrated circuit is to drive circuits at an optimal gate voltage under consideration of high temperature DT operation that means the drain current must exhibit almost zero variation with elevated temperature. Based on these concepts, for the first time, we derived the zero temperature coefficient (ZTC) point model of a DTMOS transistor for operations at typical room temperatures to military range (25°C to 125°C).

Ⅲ. ZTC MODEL OF DTMOS

Fig. 1 shows the I_D-V_G transfer characteristics with ZTC point under DT and normal mode, respectively. Compared to normal mode, the lower V_g(ZTC) with higher overdrive current of DT mode verifies that DT technology could operate in a stable circuit with lower supply voltage for low power consumption requirements. The main reason of higher overdrive current under DT mode could be attributed to its lower threshold voltage with higher mobility effect than normal mode, as shown in Fig. 2.

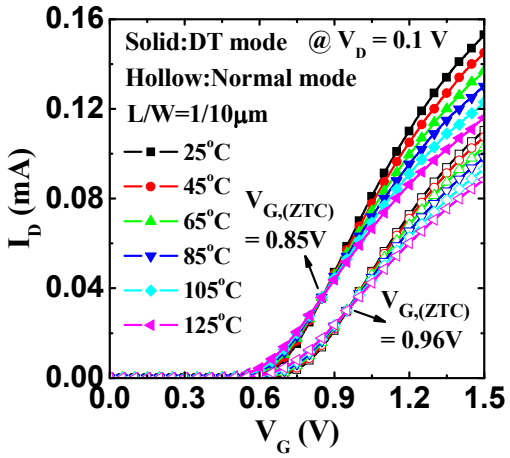

Fig. 1 I_D-V_G transfer characteristics with ZTC point at elevated temperature under DT and normal mode, respectively.

In order to accurately express the ZTC point analytical solutions for DTMOS, employing an appropriate analytical drain current model is important. As a result, our DTMOS ZTC point theory is based on the simple and accurate charge sheet approximation of the MOSFET drain current model with depletion approximation which considers both the linear and saturate regions by simultaneously including the channel potential and body effect [7].

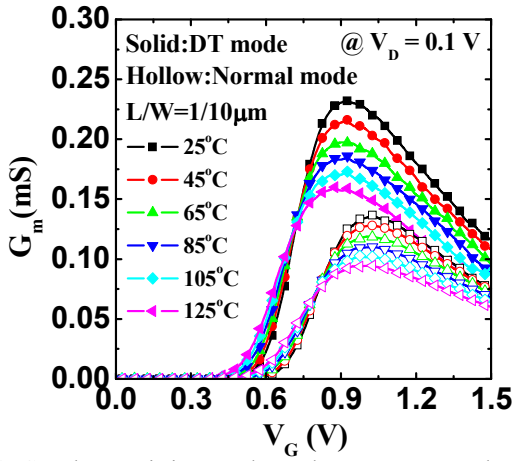

Fig. 2 G_m characteristics at elevated temperature under DT and normal mode, respectively.

For DTMOS, the drain current expressions may be expressed as

Linear region:

$$I_{DS} = \frac{W}{L} C_{ox}\mu_n \left\{ (V_G - V_T(V_{BS}))V_{DS} - \frac{m}{2} V_{DS}^2 \right\} \quad (1)$$

Saturation region:

$$I_{DS} = \frac{W}{L} C_{ox}\mu_n \frac{(V_G - V_T(V_{BS}))^2}{m} \quad (2)$$

Where

$$m = 1 + \delta \quad (3)$$

$$\delta = -\frac{dV_T}{dV_{BS}} = \frac{1}{C_{ox}} \sqrt{\frac{q\varepsilon_{Si} N_a}{2(2\phi_{fp} - V_{BS})}} \quad (4)$$

m is the body effect coefficient, C_{ox} is the gate oxide capacitance per unit area, μ_n is the effective channel mobility, and W and L are the channel width and length, respectively.

For an ideal MOS transistor, the temperature dependence of the effective mobility, is usually given as:

$$\mu_n(T) = \mu_n(T_i)\left(\frac{T}{T_i}\right)^{-K_1} \quad (5)$$

Where T_i is the initial room absolute temperature and K_1 is the corresponding constant, smaller than the previous reports, K_1 is 1.2 and 1.05 in our DT and normal mode operated transistor, respectively, which is extracted from the transconductance degradation of ZTC point at elevated operation temperature as shown in Fig. 2.

It should be noted that, because the DTMOS transistors are operated by connecting the gate with the substrate, the substrate bias may thus be given as:

$$V_{BS} = \alpha V_G \quad (6)$$

The α is defined as a constant ratio of the dynamical biases between the gate and the substrate. In our experiment, $\alpha = 0.4$ is used to validate the ZTC model accuracy of DTMOS.

The assumptions of threshold voltage dependence on temperature and body bias are modeled simultaneously in the following approximate expressions:

$$V_T(T, V_{BS}) \cong p_0 T + r_0 V_{BS} + q_0 \quad (7)$$

where

$$p_0 = \left.\frac{dV_T}{dT}\right|_{T_i \sim T_f, V_{BS} < 0.6V} \quad (8)$$

$$r_0 = \left.\frac{(V_T(T, V_{BS}) - q_0 - p_0 T)}{V_{BS}}\right|_{T_i \sim T_f, V_{BS} < 0.6V} \quad (9)$$

$$q_0 = V_T(T_i, V_{BS}) - r_0 V_{BS} - T_i \left.\frac{dV_T}{dT}\right|_{T=T_i, V_{BS} < 0.6V} \quad (10)$$

The p_0, q_0 and r_0 are average values extracted from the experimental data, as shown in Fig. 3. Further, the temperature dependence of the body effect coefficient may be approximated by the expression:

$$m = 1 + \delta \cong 1 + sT + t \quad (11)$$

where

$$s = \left.\frac{d\delta}{dT}\right|_{T_i \sim T_f} \quad (12)$$

$$t = \delta(T_i) - T_i \left.\frac{d\delta}{dT}\right|_{T=T_i} \quad (13)$$

The definition of ZTC point is given as $dI_{DS}/dT=0$. By substituting the assumptions described by equations (5)-(13) into the definition and using the least-squares method to ensure drain current independence over the temperature range T_i to T_f [5]. Consequently, by solving the equations, we propose formulations for the linear and saturation region of the ZTC point model of the DTMOS transistor:
Linear region:

$$V_T(ZTC) = \frac{\left(p_0 + \frac{sV_{DS}}{2}\right)\left(1 - \frac{1}{K_1}\right)(T_i + T_f) + V_{DS}(1 + t) + 2q_0}{2(1 - \alpha r_0)} \quad (14a)$$

Saturation region:

$$V_T(ZTC) = \frac{p_0\left(\frac{K_1 - 1}{K_1 + 1}\right)(T_i + T_f) + 2q_0 - \frac{p_0 T_\delta}{K_1}\left(\frac{4}{K_1 + 1}\right)\left[1 - \frac{T_\delta}{(T_f - T_i)}\ln\left(\frac{T_f + T_\delta}{T_i + T_\delta}\right)\right]}{2(1 - \alpha r_0)} \quad (14b)$$

where

$$T_\delta = \frac{K_1(1 + t)}{s(1 + K_1)} \quad (15)$$

Ⅳ. MODELING VERIFICATION

The proposed DTMOS ZTC model is verified using the experimental data obtained from our DTMOS device in which channel length and width is 1 and 10 μm, respectively. Due to the threshold voltage dependences on the temperature from 25°C to 125°C with different body biases, the physical parameters p_0, q_0, and r_0 of the ZTC point model for DTMOS can be extracted easily from our model, as shown in Figure 3. In general, the increased positive body bias and the increase in N_i with increasing operating temperature result in the lower threshold voltage while operated in DT mode.

The predicted value of the ZTC point model and the experimental data from our DTMOS transistor in both linear and saturation regions are shown in Fig. 4. The characteristic features s_0 and t_0 in our ZTC point model of DTMOS are extracted from the slope and extrapolated point of a body effect coefficient versus absolute temperature curve, simultaneously. The s_0 and t_0 is 0.0005/K and -0.2198 in our device, respectively. Estimations of the disagreement between DTMOS ZTC model and experimental data, roughly 0.87% in the linear region and 2.35% in the saturation region, are obtained. Similar to the conventional mosfet, the V_g(ZTC) point of DTMOS is independent of V_{DS} while operated in the saturation region. Our proposed model gives results sufficiently accurate to predict the ZTC behaviors of DTMOS.

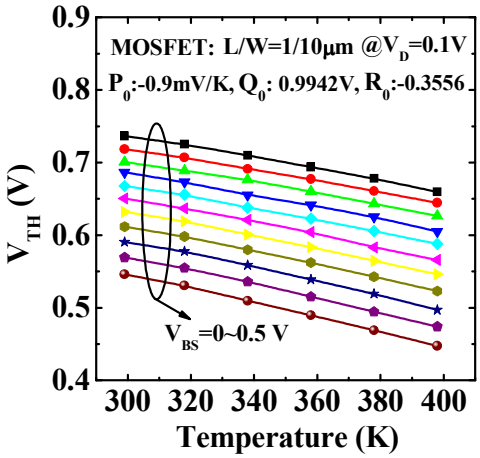

Fig. 3 Temperature dependence of the threshold voltage with different body biases at elevated temperatures from 298K to 398K.

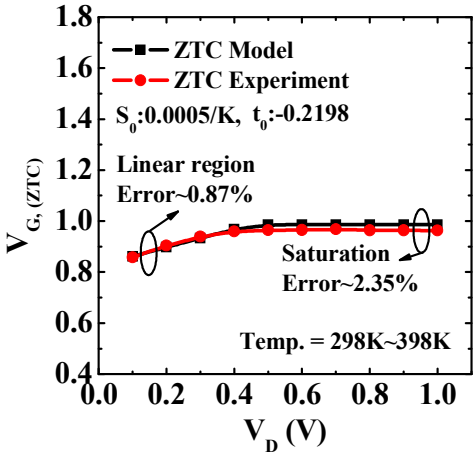

Fig. 4 The theoretical values of the ZTC point model and actual experimental data of the DTMOS transistor in both the linear and saturation regions.

Ⅴ. CONCLUSION

Analytical expressions of zero temperature coefficient (ZTC) point modeling of DTMOS transistor are successfully presented in detail. The maximum error of 0.87% and 2.35% in the linear and saturation regions, respectively, confirms the good agreement between our DTMOS ZTC point model and experimental data. The proposed formulations are simple and accurate enough to predict the ZTC point in both the linear and saturation regions, useful for future integrated circuit design using DT technology.

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