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A Simple Model for Threshold Voltage of Surrounding-gate MOSFETs With Interface Trapped Charges

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1. Introduction

When the device pushed into deep-submicrometer regime, the hot-carrier effects (HCEs) will degrade the device behavior[. Until now, the hot-carrier effects induced the threshold voltage degradation is not comprehensively studied. The surrounding-gate MOSFETs showing the better packing density and scaling length than both planar and double-gate MOSFETs are more promising for the future VLSI circuits[1]. Further exploitation and use of surrounding-gate MOSFETs in circuits require physics-based transistor model. In this paper, by considering the effects of equivalent oxide charges induced by interface trapped charges on the flat-band voltage[2], we develop the analytical threshold voltage model for the surrounding-gate MOSFETs with interface trapped charges based on scaling theory[3] and perimeter-weighted-sum method[4]. The proposed model is verified by the numerical simulation [5] and explicitly illustrates how various change conditio device structure parameters affect the threshold voltage. The findings of the model is much useful to investigate the HCEs and the design of the charge-trapped memory device.

2. Model Derivation

The surrounding-agte MOSFET is genuinely composed of double-gate MOSFETs and cylindrical MOSFET. Based on scaling theory, the central potential $\Phi_{c,i}(z)$ together with natural length of should satisfy the scaling equation

$$\frac{d^2\Phi_{c,i}(z)}{dz^2}-\frac{1}{l^2}(\Phi_{c,i}(z)-f_i)=0 \quad (i=1,2,\ and\ 3) \tag{1}$$

with

$$\frac{1}{l^2}=\frac{8C_{OX1}}{4t_{si}e_{si}+C_{OX1}t_{si}^2} \tag{2}$$

$$f_i=V_{gs}-V_{fb,i}-\frac{qN_at_{si}}{2C_{OX1}}-\frac{qN_at_{si}^2}{8e_{si}} \tag{3}$$

for double-gate MOSFETs, and

$$\frac{1}{l^2}=\frac{16C_{OX2}}{4t_{si}e_{si}+C_{OX2}t_{si}^2} \tag{4}$$

$$f_i=V_{gs}-V_{fb,i}-\frac{qN_at_{si}}{4C_{OX2}}-\frac{qN_at_{si}^2}{16e_{si}} \tag{5}$$

for cylindrical MOSFETs. Where f_i is central potential for the long-channel device, and $V_{fb,1}=V_{fb,3}$ is the flat-band

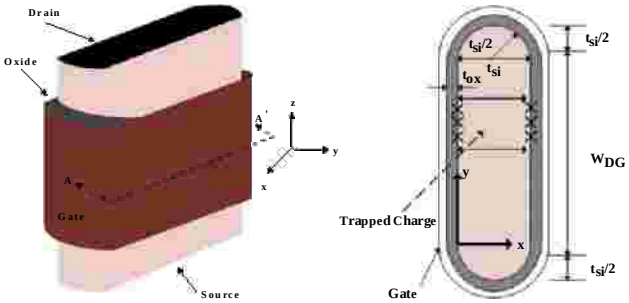

Fig. 1 Schematic of surrounding-gate MOSFETs: (a) three-dimensional device structure, (b) two-dimensional device structure to derive the model. Regions 1, 2, and 3 denote low field region near source, high field region with damage and h field region without damage.

voltage in undamaged regions. In damaged region, due to the effect of equivalent oxide charges on the flat-band voltage, we obtain

$$V_{fb,2}=V_{fb,1}-\frac{1}{C_{ox}}[\int_0^{t_{ox}}\frac{xr(x)}{t_{ox}}dx+Q_{it}]=V_{fb,1}-\frac{qN_f}{C_{ox}} \tag{6}$$

where r(x) is localized oxide charge density assumed zero for simplicity and $Q_{it}=qN_f$ is the uniform interface charge sheet density. C_{ox} can be either C_{ox1} or C_{ox2} for double-gate and cylindrical MOSFETs, which have been defined in the previous literatures[3]. The general solution of (1) can be obtained as

$$\Phi_{c,i}(z)=a_ie^{\frac{1}{l}z}+b_ie^{-\frac{1}{l}z}+f_i \tag{7}$$

Therefore, the minimum central potential can be expressed as

$$\Phi_{c,i,\min}=2\sqrt{a_ib_i}+\phi_i \tag{8}$$

By setting $\Phi_{c,i,\min}=2\phi_B$ and solving for the V_{gs} in (8), one can obtain the threshold voltage.

$$V_{th,DG,i}=V_{fb,i}+\frac{qN_at_{si}}{2C_{OX1}}+\frac{qN_at_{si}^2}{8e_{si}}-\frac{B_i+\sqrt{B_i^2-A_iC_i}}{A_i} \tag{9}$$

for double-gate MOSFETs, and

$$V_{th,CYL,i}=V_{fb,i}+\frac{qN_at_{si}}{4C_{OX2}}+\frac{qN_at_{si}^2}{16e_{si}}-\frac{B_i+\sqrt{B_i^2-A_iC_i}}{A_i} \tag{10}$$

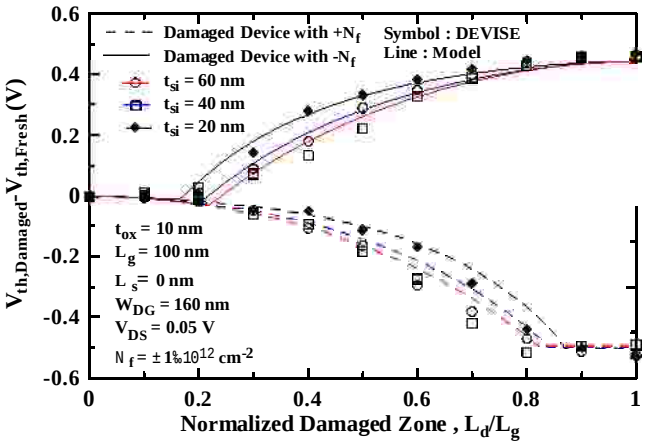

Fig. 2 Threshold voltage degradation versus normalized damaged zone for different diameters of silicon body.

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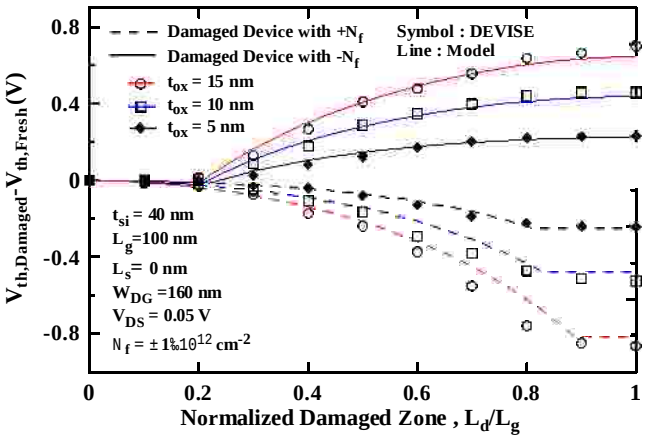

Fig. 3 Threshold voltage degradation versus normalized damaged zone for different oxide thicknesses.

for cylindrical MOSFETs. The largest value in (9) of $V_{th,DG,i}$ and in (10) of $V_{th,CYL,i}$ will dominate the threshold voltage (all of A_i,B_i,C_i are summarized in appendix). Finally, with the perimeter-weighted-sum method, the threshold voltage for the surrounding-gate can be obtained as

$$V_{th,i} = V_{th,DG,i} \times a_{DG} + V_{th,CYL,i} \times (1 - a_{DG}) \quad \text{(i=1,2, and 3)} \quad (11)$$

with

$$a_{DG} = \frac{2W_{DG}}{2W_{DG} + p\,t_{si}} \quad (12)$$

where a_{DG} is the ratio of perimeter of double-gate MOSFETs to that of surrounding-gate MOSFETs , which can be 1 (if W_{DG} >> pt_{si}) for pure double-gate device and 0 (if W_{DG} << pt_{si}) for genuine cylindrical MOSFETs.

3. Results and discussion

"*Devise*", the three-dimensional device simulator, is used to verify the proposed model. The threshold voltage is read when the electron concentration at the position of the minimum central potential is equal to the bulk doping density. For the fixed positive/negative interface sheet charge density, Fig. 2 shows how threshold voltage degradation is affected by the normalized damaged zone for different diameters of silicon body. The increased damaged zone can further degrade the threshold voltage because the interface positive/negative trapped charges will decreased/increased the flat band voltage and result in the degradation of the threshold voltage. This *interface trapped charge induced threshold voltage degradation* is so-called "ITTVD". For the positive localized interface charges, the small diameter of silicon body of t_{si}*=20 nm* will suffer less ITTVD in comparison to large diameter of t_{si}*=60 nm* when L_d is increased. On the contrary, for the negative charges, the large diameter of silicon body of t_{si}*=60 nm* will undergo less ITTVD when compared to small diameter of t_{si}*=20 nm*. Although the thinner silicon body is preferred to resist ITTVD caused by positive charges, the silicon had better become thicker not only to put up with ITTVD resulted from the negative charge, but also enhance the current driving capability. Fig. 3 shows the variation of threshold voltage degradation with the normalized damaged zone for different oxide thicknesses. To resist the ITTVD, not only thin oxide should be accounted for, but also the small damaged zone must be desired for the device. Note that when the gate oxide thickness is reduced below 10 nm, the gate leakage current caused by tunneling effects will deteriorate the device performance. The trade-off about keeping the low threshold voltage degradation without the large gate leakage current should be seriously considered in designing the device.

4. Conclusions

A simple threshold voltage model for surrounding-gate MOSFETs with interface charge-trapped is successfully developed. The model is verified by the three-dimensional simulation results and can be efficiently to explore the threshold voltage behavior for the charge-trapped memory device.

References

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