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A Forward Body Bias Characterization for Low Voltage CMOS Circuits

Hitoshi Aoki*, Masanori Shimasue*, Masaya Miyahara** and Akira Matsuzawa**

*MODECH Inc., 25-6, Yokoyama-Cho, Hachioji-Shi, Tokyo 192-0081, Japan.
Phone: +81-42-656-3360 Fax: +81-42-656-3361 E-mail: h.aoki@modech.co.jp
**Department of Physical Electronics, Tokyo Institute of Technology
2-12-1-S3-27, Ookayama, Meguro-Ku, Tokyo 152-8552, Japan. Phone/Fax: +81-3-5734-3764

1. Abstract

This paper proposes a modified transistor model to improve the accuracy under the forward body bias operation that is vital for low voltage circuits, such as 0.5 V, to reduce the power consumption of CMOS LSI. The proposed model and equations were implemented in BSIM4 version 4.6 with SPICE3f5 and verified by measurements of 90 nm NMOS transistors. About 20 % inaccuracy of the drain current can be corrected, further more the importance of the proposed model will become higher with further technology scaling.

2. Introduction

In order to reduce power dissipation while keeping speed of any circuits in battery supplied portable systems, the importance of low voltage sub-100 nm CMOS technology is increasing. However, the major problem is that the threshold voltages of n-MOSFETs cannot be monotonically scaled whereas p-MOSFETs can. To reduce the threshold voltage, we used 90 nm CMOS devices at forward body biases [1]-[3] to design CMOS circuits.

During our circuit design process, we found that the existing MOSFET compact models, such as BSIM3, 4, and HiSIM2 models, don't make sufficient attention to the forward body bias operations. In particular the simulated drain current of NMOS by the circuit simulator is much lower than the measured value under the forward body bias condition. The maximum error is about 20 % that can't be negligible to design current mixed signal circuits. Therefore we investigated the threshold voltage, V_{th}, and velocity saturation dependencies on body biases in this study and propose modified model to BSIM4 [4] as an instance for simulating drain current from reverse to forward body bias ranges.

3. Modeling and Characterizations

a) Threshold voltage

Based on our analysis and experiments, physical formulations of threshold voltages and mobility reduction due to the velocity saturation region have been analyzed, extensively when the forward body bias, V_b, was supplied.

Since the forward bias reduces the depletion region width, X_{dep}, V_{th} has a strong dependency on V_b, which is dominated by Halo implant [3]. The forward V_b dependency of X_{dep} can be written as a non-uniform vertical doping model in (1).

$$X_{dep} = \sqrt{\frac{2.0 \cdot \varepsilon_{si}\left(\phi_s - \Delta\phi_{fvb} - V_b\right)}{q \cdot N_{sub}}} . \quad (1)$$

Here, ε_{si} is a dielectric constant of silicon, ϕ_s is the surface potential, q is an electric charge, and N_{sub} is the substrate doping concentration. The newly added term is $\Delta\phi_{fvb}$ that represents surface potential reduction induced by forward body voltage. The result V_{th} has been modified accordingly.

Figure 1 shows V_{th} vs. V_{bs} characteristic of measurement and simulations used by current BSIM4 and proposed models. It shows that the simulated V_{th} by current BSIM4 has some difference under the forward bias condition, in contrast, our proposed model agreed with the measured V_{th} in sufficient accuracy.

b) Saturation drain current

In the saturation region, bulk charge effect, $A_{bulk,}$ in the saturation drain current, I_{ds}, (2) of BSIM4 needs to be modified as (3) to express the reduction of velocity saturation, v_{sat}, at the forward body biases.

$$I_{ds} = WC_{ox}\left(V_{gst} - A_{bulk}V_{dsat}\right)v_{sat} . \quad (2)$$

$$A_{bulk} = \left[1 + F_{dope}\left(F_{length} + F_{width}\right)\right] \cdot \frac{1}{R_{fvb} + K_{eta} \cdot V_b} . \quad (3)$$

Here, W, C_{ox}, V_{gst}, and V_{dsat}, are the channel width, oxide capacitance, gate-to-source voltage minus V_{th}, and saturation voltage, respectively. F_{dope}, F_{length}, and F_{width} are the functions of non-uniform doping, channel length, and channel width dependencies, respectively. R_{fvb} is the newly added parameter to represent reverse-to-forward V_b dependencies to work with K_{eta}, which is a fitting parameter in BSIM4 model.

The modified model was implemented into SPICE3f5 and all parameters were extracted from measured data. Figure 2 shows I_{ds} vs. V_{ds} with some V_{gs} voltages under the reverse bias condition for measured and simulated current by BSIM4 and our proposed models. Both of simulated currents show equivalent accuracies. Figure 3 shows I_{ds} vs. V_{ds} with some V_{gs} voltages under the forward bias condition. The simulated current by BSIM4 is much lower than that of measured value, particularly in high V_{gs} region. However, simulated current by proposed model agrees with measured data in sufficient accuracy. Figure 4 shows the saturation current I_{dsat} as a function of channel length when V_{ds} and V_{gs} are set to 1 V and V_b is 0.5 V. The simulated current by BSIM4 is lower than measured current even at larger channel length, hereby the error reaches about 20 % at the channel length of 100 nm.

The forward bias technique needs to be used for low voltage operations, such as 0.75 V or 0.5 V, to reduce the threshold voltage in more scaled devices whose electrical fields become higher. We predict the I_{ds} under the forward

bias condition for more scaled CMOS transistors in figure 5. As the inaccuracies of BSIM4 become larger with technology scaling, the proposed model will be more important.

4. Conclusions

The forward body bias technique will be important for low voltage operation such as 0.5 V, however current MOSFET compact models, such as BSIM4, don't have sufficient accuracy in this body bias operation. Its simulated drain current is about 20 % lower than the measurement. Thus we proposed modified model and equations to implement in BSIM4 version 4.6 as an instance. The estimated error can be suppressed sufficiently and we are going to complete physical model equations to simulate transistor characteristic in reverse-to-forward V_b biases.

References

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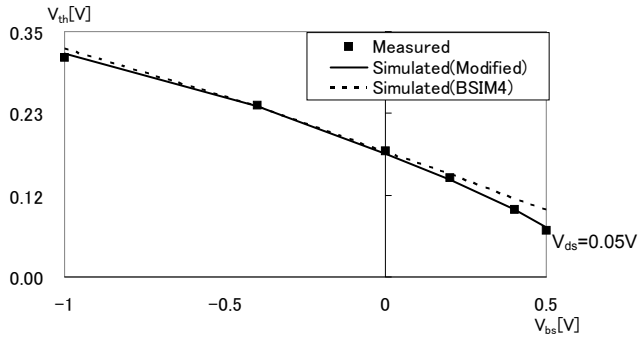

Fig. 1. V_{th}, dependencies on reverse-to-forward body biases. Here, V_{th} was adopted by the V_{gs} at the I_{ds} of 100 nA × W/L. L = 0.25 μm, W = 3.0 μm.

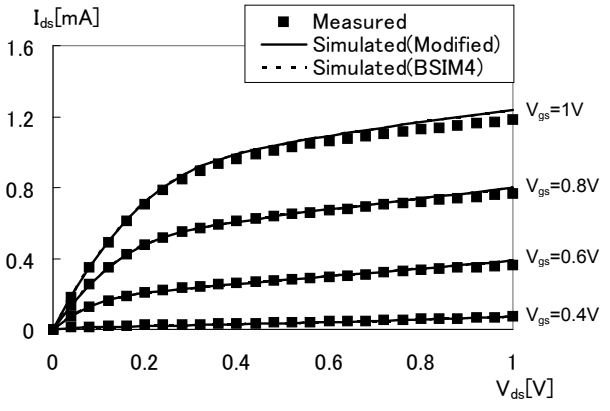

Fig. 2. Characteristic of measured and simulated I_{ds} versus V_{ds} at V_b = -1.0 V (reverse biased). Gate channel length, L, and W are 90.0 nm, and 2.0 μm.

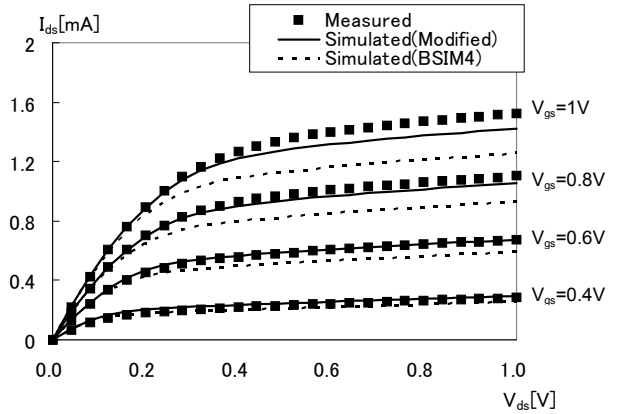

Fig. 3. Characteristic of measured and simulated I_{ds} versus V_{ds} at V_b = 0.5 V (forward biased). Gate channel length, L, and gate channel width, W are 90.0 nm and 2.0 μm.

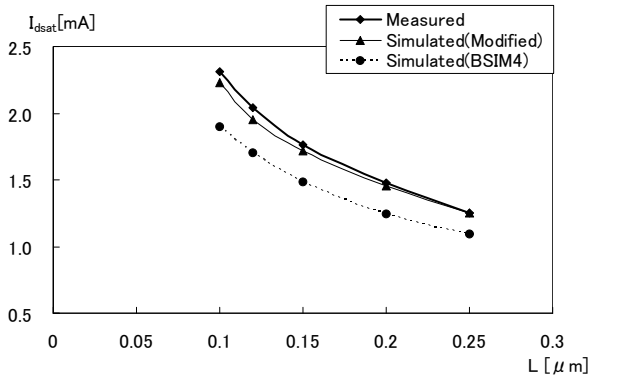

Fig. 4. Saturation current, I_{dsat}, dependencies on channel length (W = 3.0 μm). Here, I_{dsat} was obtained at V_{DD} = V_{gs} = 1.0 V and V_b = 0.5 V.

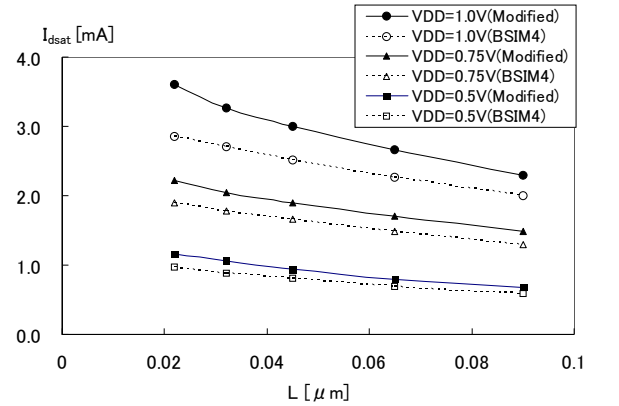

Fig. 5. Predictive simulations for shorter channel length devices (W = 3.0 μm). Here, V_{gs} is equals to V_{DD} and V_b was fixed to 0.5 V. Model parameters were extracted by T-CAD simulations.