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The Effects of Quantum Confinement on Electrical Characteristics of 12-nm Silicon-on-Insulator (SOI) FinFETs by Quantum Transport Analysis

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1. Introduction

As the channel length of MOSFETs scale down to nanoscale, the short channel effects (SCEs) become so detrimental that the conventional bulk structure shows poor electrical performance. To improve the gate control over channel, multiple-gate MOSFETs or FinFETs are investigated [1-5] and have a great possibility to be used in the 22 nm and below VLSI technology node. Furthermore, silicon-on-insulator (SOI) FinFET structure has been considered as the ultimate structure for future VLSI devices. In this kind of structure, however, quantum confinement of the channel cross section is significant and must be taken into account precisely. On the other hand, the channel length is approaching to the wavelength of electron so that the carrier transport should be also treated quantum mechanically. We recently developed a new quantum transport simulator, Schrödinger equation Monte Carlo-3D (SEMC-3D), which can handle 3D MOSFET geometry and take scattering and 2D quantum confinement into account [6]. Most previous studies on quantum transport simulation of nanowire (NW) MOSFETs focused on the ballistic limit [7-10]. In this paper, we apply SEMC-3D to examine the effects of varying-degree quantum confinement combining with scattering on the electrical characteristics of 12nm SOI FinFETs.

2. The Schrödinger Equation Monte Carlo-3D

Basically, the Schrödinger equation Monte Carlo (SEMC) approach is a variation of non-equilibrium Green's function (NEGF) method with particular treatment on scattering. The benchmark between SEMC and the well known NEGF simulator NANOMOS [11,12] had been done in the ballistic limit and the results showed excellent agreement [13]. The schematic diagram of how scattering is treated in SEMC is shown in Fig. 1 which contains one initial state and hundreds of final states. The Schrödinger equation for initial state is

$$[H_i(\mathbf{r}) - E]\psi_i(\mathbf{r}) + \sum_{q=1}^{Q} M_q(\mathbf{r})\psi_{f,q}(\mathbf{r}) = \mathrm{A}(\mathbf{r}) \quad (1)$$

For each final state, the Schrödinger equation is

$$[H_f(\mathbf{r}) - E]\psi_{f,q}(\mathbf{r}) + M_q^*(\mathbf{r})\psi_i(\mathbf{r}) = 0 \quad (2)$$

In (1) and (2), $\mathbf{r}$ represents the carrier coordinate in real space. $\psi_i(\mathbf{r})$ and $\psi_{f,q}(\mathbf{r})$ represent the initial state and one of the final states, respectively. $H_i(\mathbf{r})$ and $H_f(\mathbf{r})$ are the Hamiltonians for the carrier in initial state and final state, respectively. $M_q(\mathbf{r})$ is the coupling potential between the initial state and a final state. $\mathrm{A}(\mathbf{r})$ is the artificial source term representing injection into the simulation region via the carrier coordinates or injection via a known prior state. (1) and (2) are solved for the initial and final states in 1D, i.e., $\mathbf{r}$ is replaced by x, and served as the transport equations for SEMC-3D. Fig. 2 is the flowchart of SEMC-3D. The formation of subbands due to 2D quantum confinement of channel cross section can be obtained by solving 2D Schrödinger equation of each slice along the channel

$$\left[-\left(\frac{\hbar}{2m_{y,v}}\frac{\partial^2}{\partial y^2} + \frac{\hbar}{2m_{z,v}}\frac{\partial^2}{\partial z^2}\right) + V_x(y,z)\right]\varphi_{n,v,x}(y,z) = E_{n,v,x}\varphi_{n,v,x}(y,z) \quad (3)$$

where the subscript n stands for the n^{th} eigenstate, the subscript v stands for the v^{th} valley, and the subscript x stands for the position along the transport direction. The electrostatic self-consistency is achieved by solving 3D Poisson equation for each iteration. More details about SEMC approach and SEMC-3D can be found in [6,13].

Fig. 3 shows the simulated SOI FinFET structure. Fig. 4 shows the three simulated fin cross sections with the fin height of 3nm, 4nm and 5nm. All of the simulated SOI FinFETs have 12nm gate length, 4nm fin width, 1nm gate oxide thickness, and 5nm source and drain regions. Note that the gate length is the triple of the fin width to ensure the immunity to SCEs and the validity of decoupling confinement and transport directions. The doping concentration in the source and drain regions is n-type 10^{20} cm^{-3} and the channel region is undoped. For simplicity, the work-function difference between the metal gate and the underlying Si channel is assumed to be zero. 20 subbands are considered, and the scattering processes included in the simulation are inter- and intra- valley acoustic and optical phonon scatterings. The channel orientation is <100>.

3. Results and Discussion

Fig. 5 shows the I_D-V_G curves of the SOI FinFET with 4nm fin height in ballistic and with scattering cases. The drain current is defined by the current through the device divided by the fin periphery, so the unit is A/m. The degradation of the drain current and transconductance due to scattering is significant (about 33% reduction of I_{ON} which is defined by the drain current under $V_G = V_D = 0.4$V) even at 12nm gate length. Figs. 6(a) and (b) show the I_D-V_G curves of the SOI FinFETs with 3, 4 and 5nm fin height in the ballistic limit and under scattering, respectively. In the ballistic case, the drain currents (in nA/nm) of different fin height are almost the same which implies that the total current through the device will be proportional to the fin periphery according to our definition. However, when scattering is included, the I_{ON} of 5nm fin height device is about 7% higher than those of 3 and 4nm fin height devices. To explain this phenomenon, first, we examine the subbands of the SOI FinFETs. The first three subbands of the devices with varying fin heights are listed as Table I. As expected, the subbands of the device with lower fin height have higher energies. Note that as the fin height is equal to 4nm, the first subband and the second subband are degenerate due to the symmetry of the fin cross section. Fig. 7 shows the first subband profiles along the channel of different fin heights. Their barrier heights are almost the same and barrier tops are located around x = 6nm. Second, we check on the scattering rate around the barrier top which is regarded as the bottleneck of the current flow [14]. Fig. 8 shows the average scattering rate of the carriers injected from the source side (only these carriers contribute to the drain current). Around the barrier top, the scattering rate of 5nm fin height device is lower than those of 3 and 4nm fin height devices and thereby results in higher I_{ON}. The degeneracy of the first and the second subbands of the device with 4nm fin height (the fin width is also 4nm) facilitate the inter-subband (or inter-valley) scattering and thus make the scattering rate and I_{ON} close to those of the device with 3nm fin height. The carrier density distributions on the fin cross sections of varying fin heights are shown in Fig. 9. As the fin height decreases, the carriers are concentrated toward the center and thus increase the scattering rate.

4. Conclusions

Quantum transport simulation of 12nm SOI FinFETs with varying fin heights had been done by an in-house simulator, SEMC-3D. The simulation results show that the degradation of the drain current and transconductance due to scattering is still significant even at 12nm gate length. When scattering is considered, reducing the fin height, i.e., increasing the quantum confinement, will degrade I_{ON} because of increasing the scattering rate around the barrier top of the channel. The square fin cross section should be avoided since the degenerate subbands will increase the scattering rate and degrade I_{ON}.

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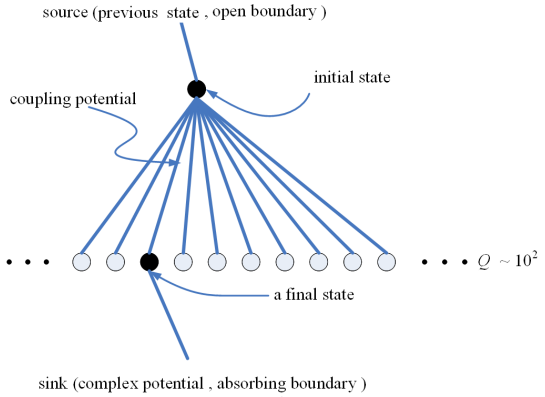

Fig. 1. Schematic representation of the way scattering is treated in SEMC. Scattering is considered by solving initial state and final states. Note that the number of final states is reduced to tens or hundreds [6].

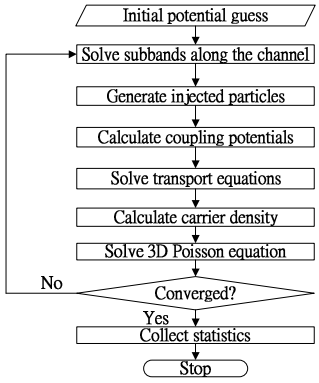

Fig. 2. Flowchart of SEMC-3D [6].

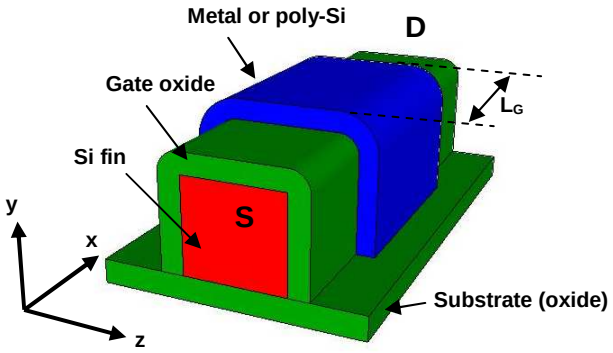

Fig. 3. The simulated SOI FinFET structure.

Table I. The first three subbands under different fin heights and 4nm fin width. The energy of conduction band edge at the source end is 0 eV.

Subband \ Fin height	3nm	4nm	5nm
E_0 (eV)	0.09480	0.08280	0.06135
E_1 (eV)	0.1313	0.08280	0.07998
E_2 (eV)	0.1880	0.1392	0.1091

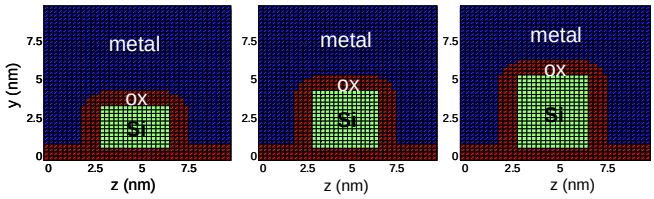

Fig. 4 The simulated fin cross sections with the fin heights of (a) 3nm, (b) 4nm, and (c) 5nm. The fin width is 4nm and the mesh is also shown.

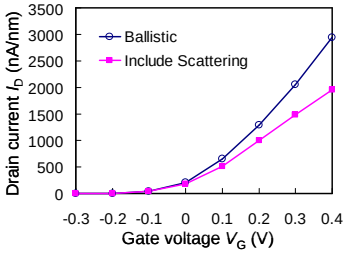

Fig. 5 The I_D-V_G curves of the SOI FinFET with 4nm fin height under V_{DD} = 0.4V in the ballistic and with scattering cases.

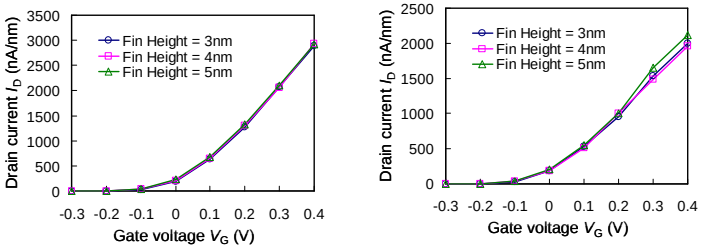

Fig. 6 The I_D-V_G curves of the SOI FinFETs with 3, 4, and 5 nm fin height under V_{DD} = 0.4V in the (a) ballistic and (b) with scattering cases.

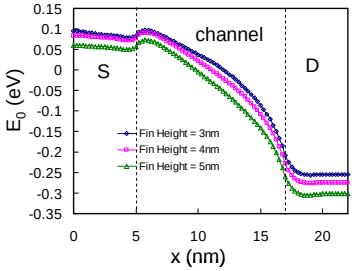

Fig. 7 Profiles of the first subband along the channel for different fin heights under $V_G = V_D$ = 0.4 V. Scattering is taken into account.

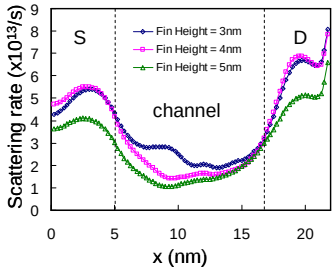

Fig. 8 Average scattering rate along the channel of the electrons injected from the source side under different fin heights. The bias condition is $V_G = V_D$ = 0.4 V.

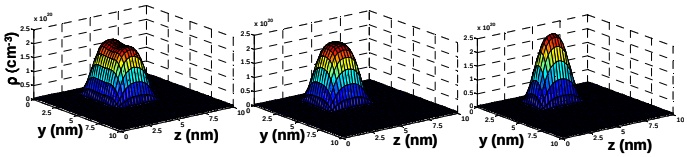

Fig. 9 Electron density distributions on the fin cross sections with the fin heights of (a) 5nm, (b) 4nm, and (c) 3nm at the source end.