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Investigation of SACVD-Based STI Process on Electrical Characteristics of Nanoscale NMOSFETs

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1. Introduction

In order to improve nanoscale CMOS device performance and to maintain Moore's Law, strain engineering has been widely adopted as a performance booster since the 90nm technology node [1]. However, the high-level of mechanical compressive stress, resulting from the conventional High Density Plasma (HDP) Shallow Trench Isolation (STI) gap filling process significantly degrades the device performance, negating the benefits of strain technologies as device active area shrinks, particularly for NMOSFETs [2]. Recently, Sub-Atmospheric Chemical Vapor Deposition (SACVD) oxide has been developed as a standard shallow trench filling process to achieve a high aspect ratio gap-fill capability and to reduce the STI-induced compressive stress at the 45-nm node [3]. Despite this, continued efforts should be made to further reduce the STI stress in advanced device structures with even smaller isolation pitches in future technologies. In this work, NMOSFETs with an improved STI densification annealing process based on SACVD oxide are demonstrated to further reduce the STI stress.

2. Experiment

NMOS devices used in this work are fabricated by state-of-the-art 40nm strained-Si technology. Fig. 1 shows the device geometric parameters. In Fig. 2, the SACVD-based STI process flow is shown. After STI patterning and wall oxidations, trenches are filled with SACVD oxide followed by two different densification annealing conditions: Standard and STI-B, where STI-B process has only half oxygen (O_2) flow during the densification anneal to reduce the STI compressive stress. Apart from the STI densification anneal process, Standard and STI-B devices are fabricated by the identical process flow. A transmission-electron-microscope (TEM) image is shown in Fig. 3. There is no appreciable distinction of active width on small device with Standard and STI-B processes.

3. Results and Discussion

I_D-V_G characteristics of 40-nm NMOSFETs with Standard and STI-B process are plotted in Fig. 4, and both kinds of devices show similar drain induced barrier lowering (*DIBL*) characteristics, subthreshold swing, and off-current (I_{OFF}). It implies that the improved densification process has no significant influences on process variations or dopant diffusions as compared to Standard devices. The layout dependences of the on-current (I_{ON}) in 40-nm Standard and STI-B devices on the source/drain length ($L_{S/D}$) and the gate width (W) are shown in Fig. 5 and Fig. 6, respectively. Due to the enhancement of electron mobility from the reduced STI-originated compressive stress, a higher on-current can be obtained in devices with STI-B process. To clarify the origin of driving current enhancement, the total resistance ($R_{tot} = R_{Channel} + R_{SD}$) versus gate length is plotted in Fig. 7, in which the carrier mobility from the reciprocal of slope can be observed [4]. It indicates that the improved anneal process (STI-B) can effectively reduce compressive stress induced by STI process. In Fig. 8, as a result of an effective reduction in the STI-induced compressive stress through the STI-B process, a significant drive current enhancement of 8% for the 40-nm devices with narrowest W and smallest $L_{S/D}$ is shown. Process simulations using Synopsys Sentaurus software have been used to get further understanding on the STI-induced stress in the active region with different densification processes as a function of the spacing between STI (Fig 9). It can be seen that the compressive stress is effectively reduced by using the STI-B process.

In Fig 10, the breakdown voltage measured from finger n-type and p-type active structures with block poly on top of it were used to evaluate the STI oxide quality. No significant discrepancy of breakdown voltage between both finger type active structures found in our case indicates that the STI-B process would not affect on active gate oxide edge reliability for devices. On the other hand, the quality of STI with the improved densification process is also evaluated by junction leakage (Fig. 11). The leakage currents in both n^+/p and p^+/n diodes with STI-B process are less than those in diodes with Standard process, and it can be attributed to the less energy bandgap narrowing induced by the lower compressive stress, further verifying that STI-B process can effectively reduce the mechanical compressive stress [5].

4. Conclusions

We have investigated and presented an improved densification process for SACVD-based STI processes in 40nm technology to effectively reduce STI-induced compressive stress and to boost NMOSFET performance. With scaling of the W and $L_{S/D}$, the performance enhancements of NMOS devices continue to increase.

Hence, the improved densification process of STI process is suitable for the small isolation pitches used in 40nm generations or beyond and without degradation the quality of STI process.

Acknowledgements

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References

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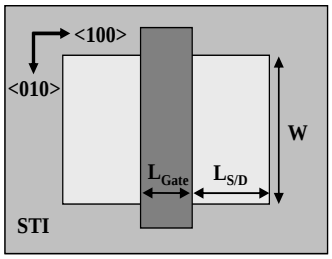

Fig.1 Schematic of the device layouts used in this work.

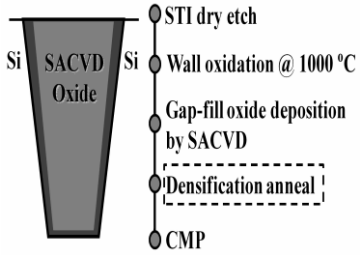

Fig.2 Schematic cross section and process flow of SACVD oxide-filled STI.

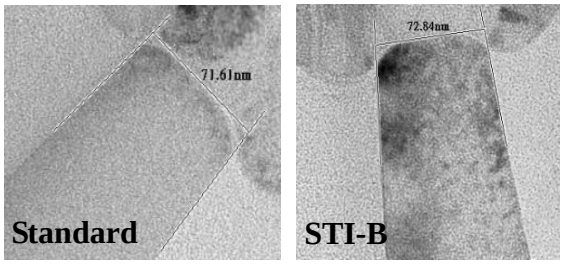

Fig. 3 TEM pictures for smaller active width with Standard and STI-B process.

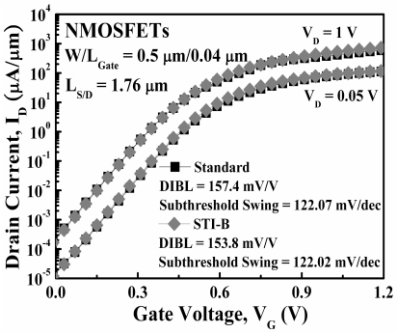

Fig. 4. I_D-V_G characteristics of NMOSFETs at a gate length of 40nm with Standard and STI-B process.

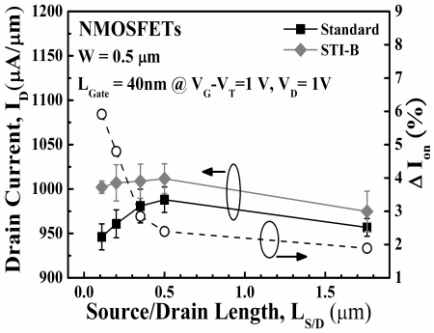

Fig.5 I_{ON} of 40-nm NMOSFETs with different STI process as a function of $L_{S/D}$.

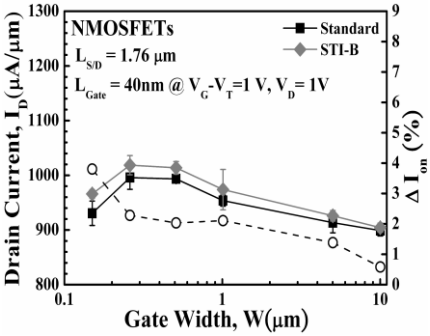

Fig.6 I_{ON} of 40-nm NMOSFETs with Standard and STI-B process as a function of *W*.

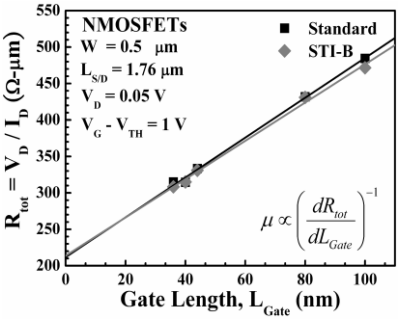

Fig. 7. Total resistance for nMOSFETs with Standard and STI-B process as function of the gate length.

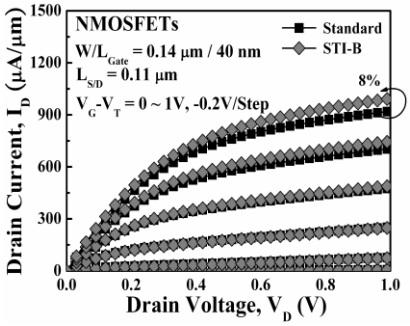

Fig.8 I_D-V_D characteristics of the 40-nm NMOSFETs with Standard and STI-B process.

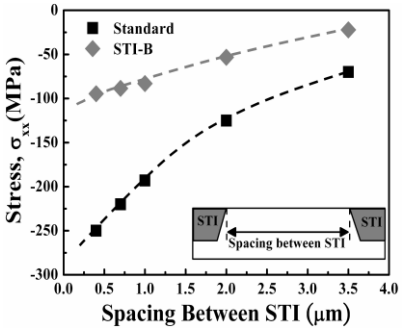

Fig. 9. Simulated STI-induced stress in the active region with Standard and STI-B densification process.

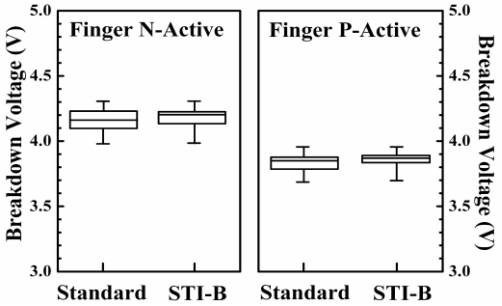

Fig. 10. The breakdown voltage of figure n-type and p-type active structure with Standard and STI-B process.

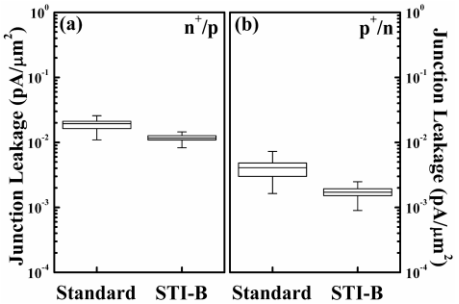

Fig. 11. The junction leakage current of (a) n^+/p and (b) p^+/n junction diodes with Standard and STI-B process.