Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp295-296

Calibration of Linear Piezo Resistance Coefficients using 3-Dimensional Stress Simulation of Si-MOSFETs Structures

[1]Akira Satoh, [1]Tetsuya Tada, [1]Vladimir Poborchii, [1]Toshihiko Kanayama,
[2]Shigeo Satoh and [1]Hiroshi Arimoto

[1]National Institute of Advanced Industrial Science and Technology
Nano-device Innovation Research Center (AIST-NIRC),
1-1-1 Higashi, Tsukuba, Ibaraki 305-8562, Japan
Phone: +81-29-849-1216 E-mail: ak-satoh@aist.go.jp
[2]Fujitsu Semiconductor Ltd. (FSL), 50 Fuchigami, Akiruno, Tokyo 197-0033, Japan

1. Introduction

Stress in the channel region of Si MOSFET is a key parameter to estimate carrier mobility in Si MOSFET using a local strain technique from the viewpoint of modeling for layout variation. Presently, the Piezo resistance model has been adapted as the carrier mobility model due to stress. However, both stress distribution and Piezo resistance coefficients in the silicon device are not quantized strictly. Therefore, dependencies of characteristics could not be reproduced on the layout of SI-MOSFETs. We demonstrated that the stress distribution of the Si-MOSFET structure could be precisely estimated by calibrating stress simulation using the polarized UV Raman spectroscopy [1].

In this paper, we report the mobility model calibration based on calibrated 3-dimensional stress simulation.

2. Piezo resistance coefficients calibration

Figure 1 schematically illustrates the top view of Si-MOSFET with several layout parameters. The layout parameters to be focused are SDW (SD width), SLX (stress liner boundary along x axis), SLY (stress liner boundary along y axis), STY (STI width along y axis) and NDY (neighbor diffusion width along y axis). These parameters affect to the stress distribution of Si-MOSFET. Figure 2 (a) and (b) compare SDW dependence comparison of the Raman shift which was measured by Raman spectroscopy under an offset spacer of Si-MOSFET and which was calculated from the stress tensor by stress simulations for a compressive SiN covered PMOSFET and a tensile SiN covered NMOSFET, respectively. Both PMOSFET and NMOSFET agree well. We have confirmed that the stress distribution obtained by stress simulation has accurately reproduced the distribution of Si-MOSFET structure.

When stress is applied in silicon crystal, carrier mobility is modified using the Piezo resistance model. Transistors were aligned along the [110] axis on the (100) Si wafer. Thus, mobility change along the x axis is expressed as follows:

$$\frac{\Delta\mu_x}{\mu_0} = \frac{\Pi_{11}+\Pi_{12}+\Pi_{44}}{2}\sigma_x + \frac{\Pi_{11}+\Pi_{12}-\Pi_{44}}{2}\sigma_y + \Pi_{12}\sigma_z \quad (1)$$

where, Π_{11}, Π_{12}, and Π_{44} are Piezo resistance coefficients of Si. σ_x, σ_y, and σ_z are stress tensor components along x//<110>, y//<-110>, and z//<001> axes, respectively.

Piezo resistance coefficients were calibrated in PMOSFET and NMOSFET. Fitting parameters of r_s and r_{44} were defined [2]. Eq. (1) was expressed using r_s and r_{44} as follows:

$$\frac{\Delta\mu_x}{\mu_0} = \frac{r_s(\Pi_{11}+\Pi_{12})+r_{44}\Pi_{44}}{2}\sigma_x + \frac{r_s(\Pi_{11}+\Pi_{12})-r_{44}\Pi_{44}}{2}\sigma_y + r_s\Pi_{12}\sigma_z \quad (2).$$

r_s and r_{44} were found by comparing measured Gm ratio with various SLX and SLY. The stresses along the x axis and y axis were controlled independently by changing SLX and SLY with the same L, W, and SD width as summarized in Table I.

3. Results and discussion

Figure 3 (a) and (b) are the calibration results for PMOSFET and NMOSFET, respectively. The values of r_s and r_{44} were 5.55 and 0.32 for PMOSFET, and 0.39 and 0.94 for NMOSFET. To compare Intel mobility model [3], the calibrated Piezo resistance model agreed well with the measured Gm ratio. For NMOSFET, all layouts agreed well. For PMOSFET, the difference became large as SD width (SDW01 and SDW02) narrowed. Figure 4 (a) and (b) show the SD width dependency of Gm ratio and mobility ratio of PMOSFET and NMOSFET, respectively. As mentioned earlier, for NMOSFET, all the SD width ranges agreed well. For PMOSFET, when SD width was less than 0.4 μm, it became more different from the Gm ratio was. Stress distribution is correct as shown Fig. 2. It is very difficult to explain with just change of stress. These differences might be caused by the parasitic resistance increasing as the SD width narrowed.

4. Conclusion

The linear Piezo resistance model was calibrated using stress tensor by a well calibrated 3-dimensional stress simulation. By using of precise stress distribution in channel region of Si-MOSFET, the calibrated mobility model could predict mobility dependencies on layout parameters of Si-MOSFET.

References

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[2] A. T. Bradley *et al.*, IEEE Trans. ED 48, (2001) , 2009.
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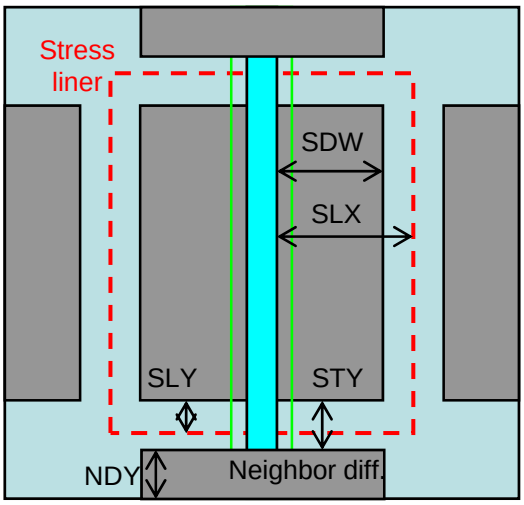

Fig. 1. Layout parameter of Si MOSFET.

Table I. Stress tensor changes of the structures for Piezo resistance coefficient calibration.

		PMOSFET			NMOSFET		
		$\Delta\sigma_x$ (%)	$\Delta\sigma_y$ (%)	$\Delta\sigma_z$ (%)	$\Delta\sigma_x$ (%)	$\Delta\sigma_y$ (%)	$\Delta\sigma_z$ (%)
SLX	0.35 (SLX01)	0	0	0	0	0	0
(μm)	5.25 (SLX02)	174	-2	3	135	0	3
SLY	0.1 (SLY01)	0	0	0	0	0	0
(μm)	0.2 (SLY02)	6	-18	-1	0	-15	-1
	0.5 (SLY03)	12	-52	0	1	-42	-2
	1 (SLY04)	14	-66	0	1	-50	-3
	5 (SLY05)	18	-83	0	-1	-60	-2

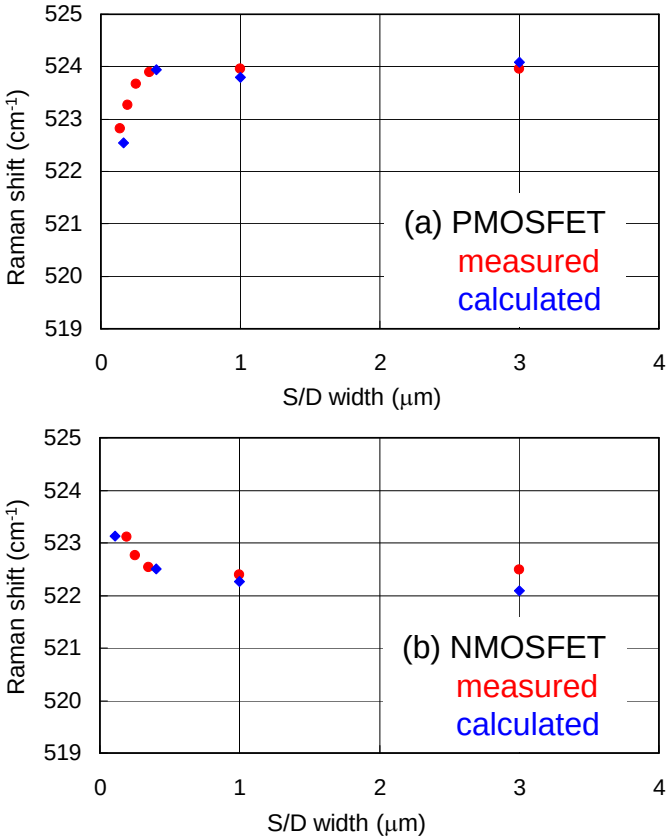

Fig. 2. SD width dependence of measured and calculated Raman shift for (a) PMOSFET and (b) NMOSFET.

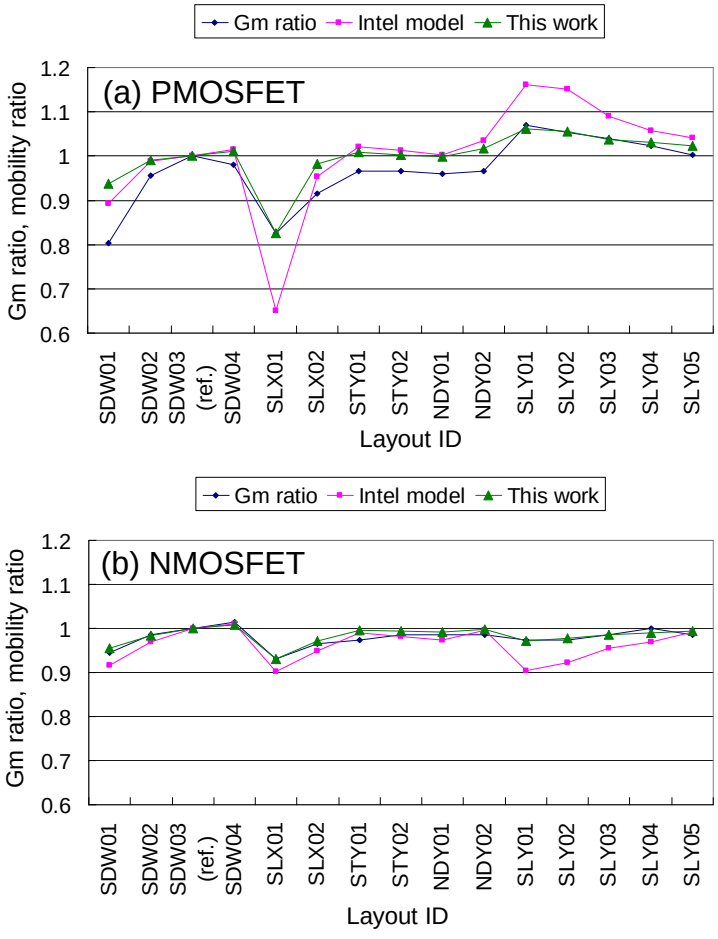

Fig. 3. Gm ratio and mobility ratio of various transistor layout for (a) PMOSFET and (b) NMOSFET.

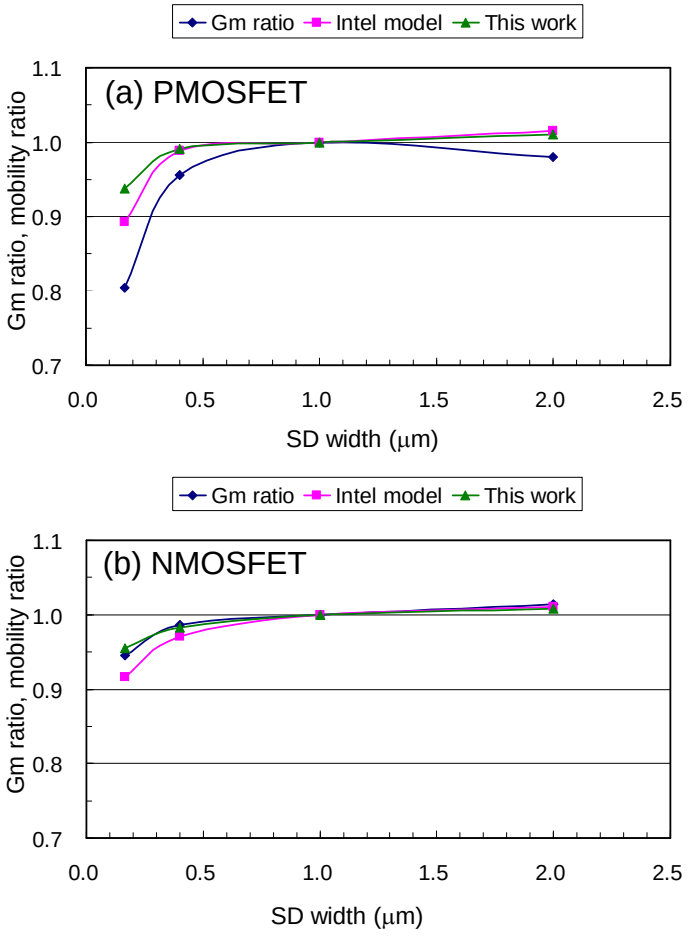

Fig. 4. SD width dependence of Gm ratio and mobility ratio for (a) PMOSFET and (b) NMOSFET.