

Investigation of Different Capping Layers and Strain Sources for SMT Process

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I. INTRODUCTION

Strain technique has emerged as a promising way for scaling down demand, including biaxial and uniaxial strain. For biaxial strain, a relaxed SiGe buffered layer fabricated by complex process may meet Ge out diffusion and dislocation penetration issues. For uniaxial strain, such as SiC S/D, contact etch-stop layer (CESL), and stress memorization technique (SMT) have been introduced.[1]-[3] Among these techniques, SMT possesses simpler process, and could be combined with other strain technique. Besides, Metal-Inserted-Poly-Si (MIPS) combined with SMT could alleviate poly-Si depletion and achieve promoted mobility.[4][5] Recently, the influence of geometrical dependence and amorphization condition on the strain coupling was thoroughly investigated, since the thermal expansion characteristics of poly-Si gate as strain source play an important role for SMT.[6] However, the impact of capping layer properties and different strain sources on SMT fabrication still needs to be clarified. In this paper, different strain sources have been analyzed. And the impact of compressive and tensile nitride on performance, gate leakage, and hot carrier immunity is completely investigate.

II. EXPERIMENT

A 30Å gate oxide was thermally grown on 6-in wafers. Poly-Si gates (2000 Å) were deposited at different temperatures, 550°C, 580°C, and 600°C, for investigating the difference of strain source. After spacer and S/D extension formation, four different silicon nitride (SiN) capping layers (1500 Å) were deposited by PECVD, modulating the flow rate of N₂ or SiH₄ as shown in Table 1 to confine the poly-Si gates. After RTA process, the S/D and poly-Si gate were activated and the channel strain was induced simultaneously. Subsequently, the capping layers were removed, leaving a memorized strain in the channel.

III. RESULT AND DISCUSSION

From thermal expansion confinement viewpoint, capping layer with higher Young's modulus could firmly confine the expanding volume of silicon gate and induce higher strain into the channel. As Young's modulus shown in Table 1, it is not consistent based on only Young's modulus viewpoint, meaning that there must be another mechanism for SMT. We observed that the initial compressive nitride possesses the highest strain coupling as well as the shift of intrinsic stress than all initial tensile capping layers as shown in Fig. 1. Therefore, it is the intrinsic stress shift of capping layer rather than initial or annealed stress that determines the quantity of strain coupling. Besides, the higher stress shift of capping layer, the higher shrinkage the film executes as shown in Fig. 2. Therefore, unlike the traditional CESL demand, the compressive layers possess promising potential for executing SMT.

Based on the strain source analyses, we found that the lower the deposition temperature for poly-Si gate, the higher the strain would be memorized after removing capping layer as shown in Fig. 3. We believe the recrystallization condition and thermal expansion coefficient of strain source are responsible for the phenomenon in our experiment. Consequently, the poly-Si deposited at lower temperature should be adopted for maximizing the strain coupling for the MIPS application.

We found that all samples made using the SMT process show a decreased interface-state than control sample. To investigate the mechanism of interface-state passivation, initial and annealed samples were measured by using Fourier transform infrared

spectroscopy (FTIR) as shown in Fig. 5-6. Previous report depicted that the initial quantity of nitride have an influence on passivating dangling bonds. [7] From initial and annealed FTIR comparison, the Si-H and N-H broke and released into the channel during the annealing process. The diluent gas affects both hydrogen of as-deposited nitride and the released hydrogen during annealing process. Therefore, the properties of interface condition with SMT process depend on not only hydrogen coupling during deposition, but also the content of hydrogen released during annealing process. Moreover, the higher hydrogen content is always accompanied with higher stress shift as well as shrinkage, meaning that we can evaluate the strain incorporation of SMT by tracing the hydrogen content in nitride. From the strain source comparison, the poly-Si gate deposited at a lower temperature has lower interface states as shown in Fig. 7. From the literature, hydrogen would tend to diffuse through S/D and laterally diffusion into the channel region rather than diffusion through silicon gate for CESL application.[8] However, we believe the diffusion through silicon gate is still important, although the grain boundary would trap hydrogen for SMT.

The gate leakage characteristics were shown in Fig. 8. The sample with compressive capping layer has a comparable performance as control. However, we found that SiH₄-high and N₂-med possess a higher gate leakage and even soft breakdown phenomenon. But, the leakage has a weak dependence on the quantity of strain coupling. Compared to the intrinsic stress, we believe the annealed stress is responsible for the degraded oxide quality. During the annealing, the stress of the capping layer increase and would degrade oxide quality subsequently. After removing capping layer, the stress would also be released; However, the stress induced damage would be remained.

Furthermore, the immunity of hot carrier has been analyzed. Devices were stressed at V_{DS}=3.5V and V_G at maximum substrate current as shown in Fig 9-10, demonstrating threshold voltage shift as a function of time for SMT with different nitrides. The N₂-med and SiH₄-high reveal the worst degradation in terms of the largest threshold voltage shift, meaning that the damaged oxide quality induced by stress of capping layer is the dominant mechanism rather than the strain coupling.

IV. CONCLUSION

We have demonstrated the stress shift of nitride is the critical role for SMT strain coupling. The degradation of oxide induced by stress is responsible for soft breakdown, gate leakage and higher threshold voltage shift under hot-carrier stressing. Therefore, we believe compressive nitride is a promising material to execute SMT based on mobility enhancement, gate leakage, and hot carrier immunity concern. Based on the result of different strain sources, the poly-Si gate deposited at a lower deposition temperature could couple a higher strain for metal-inserted-poly-Si structure application. In addition, we found that the hydrogen released during the annealing could further passivate interface states, and hydrogen diffusion from nitride through silicon gate is significant as well as laterally diffusion via S/D region.

REFERENCES

- [1] P. R. Chidambaram et al. *IEEE Trans. Electron Devices*, pp. 944, 2006.
- [2] C. Clays et al, *Solid-State Electronic*, pp. 1115, 2008.
- [3] T. Miyashishita et al., *IEDM Tech. Dig.*, pp.1, 2008
- [4] M. Goto et al., *Symp. VLSI Tech. Dig.*, pp.132, 2008

- [5] C. Auth et al., Symp. VLSI Tech. Dig., pp.128, 2008.
 [6] H. Ohta et al., IEDM Tech. Dig., pp.289, 2007
 [7] C. S. Lu et al, SSDM **2003**, 428 (2003)
 [8] C. S. Lu et al, Appl. Phys. Lett, 122110 (2007)

	N ₂ -low	N ₂ -med	N ₂ -high	SiH ₄ -high
N ₂ (sccm)	50	100	1000	100
SiH ₄ (sccm)	50	50	50	100
NH ₃ (sccm)	6	6	6	6
Initial stress(Mpa)	-215	148	477	227
Annealed Stress(Mpa)	870	910	525	1165
Young's Modulus(Gpa)	149.386	161.905	166.562	169.246

Table. 1 The flux of reactant and diluents gas for nitride deposited by PECVD. The comparison of initial stress, annealed stress, and Young's Modulus.

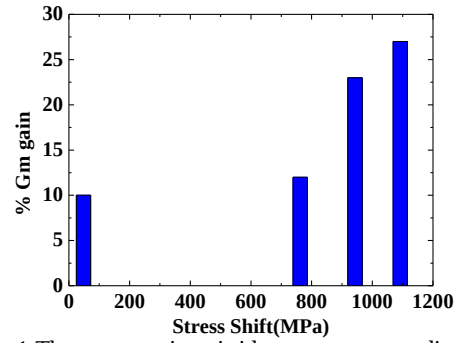


Fig. 1 The compressive nitride possess outstanding strain coupling than tensile ones for SMT process.

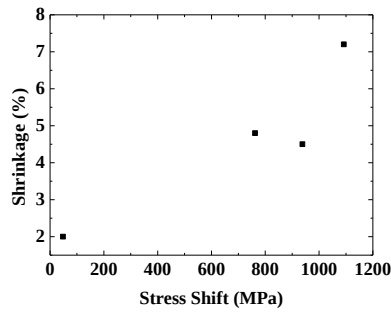


Fig. 2 The stress shift is proportional to shrinkage.

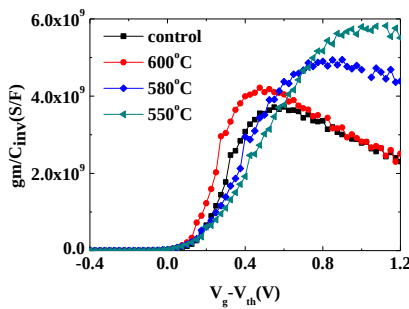


Fig. 3 The silicon gate with lower deposition temperature possesses higher strain coupling.

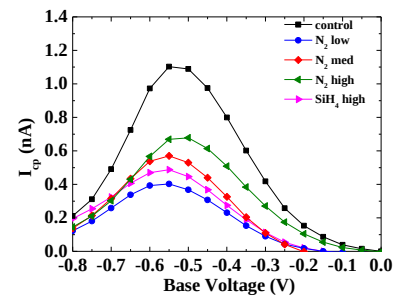


Fig. 4 All strain samples possess lower interface state than control samples.

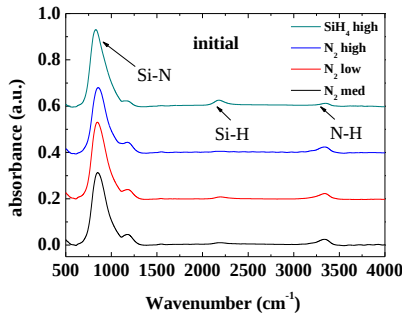


Fig. 5 Before annealing, Si-N, Si-H, and N-H of nitride was analysis by FTIR.

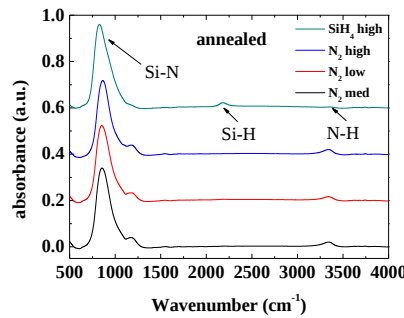


Fig. 6 After annealing, Si-N, Si-H, and N-H of nitride was analysis by FTIR.

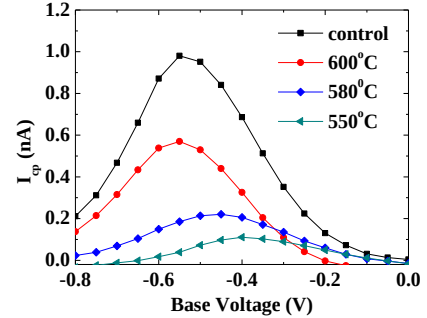


Fig. 7 The silicon gate with lower deposition temperature possesses better interface.

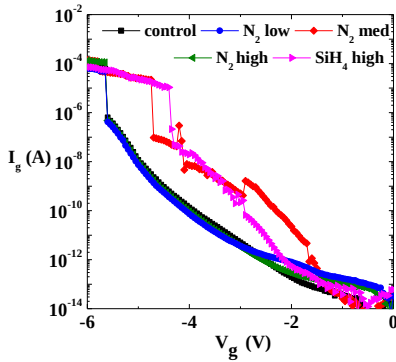


Fig. 8 The comparison of gate leakage of all samples. N₂-med and SiH₄-high reveal soft break down.

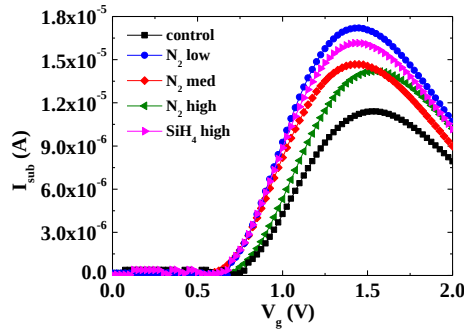


Fig. 9 The characteristics of substrate current versus gate voltage.

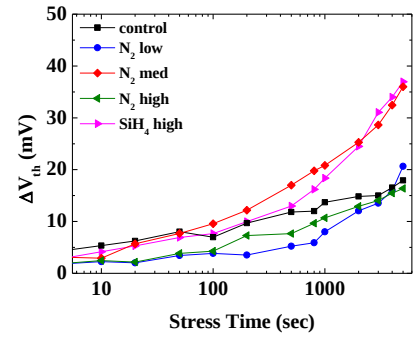


Fig. 10 Threshold Voltage shift as a function of stress time. Devices was stressed at V_{DS}=3.5V, and V_G of maximum substrate current.